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SOLID STATE MICROWAVE RECTIFICATION

Paul H. Smith
Network Instruments

TECHNICAL REPORT NO. RADC-TR-67-304
July 1967

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Paul H. Smith
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FOREWORD

This final report was prepared by Paul H. Smith of Motorola Incorporated, Semiconductor Products Division, 5005 East Mc Dowell Road, Phoenix, Arizona, under Contract AF30(602)-4119, project number 5573, task number 557305. Secondary report number is G-29. RADC project engineer is R. H. Chilton (EMATE).

This technical report has been reviewed by the Foreign Disclosure Policy Office (EMLI). It is not releasable to the Clearinghouse for Federal Scientific and Technical Information because it contains information embargoed from release to Sino-Soviet Bloc Countries by AFR 400-10, "Strategic Trade Control Program."

This report has been reviewed and is approved.

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ABSTRACT

The purpose of this contract was to investigate the problem of high efficiency microwave rectification with hot carrier diodes and to provide diodes having the highest efficiency possible in the frequency range of 3 to 8 GHz. A theoretical analysis is first made of the problem from the circuit viewpoint in an effort to determine which rectifier configurations should produce optimum efficiency, assuming perfect diodes. This is followed by an analysis of the losses to be expected for various circuits on the basis of a given diode equivalent circuit. Details of diode design, fabrication and characterization are followed by low and intermediate frequency efficiency measurements, where an attempt to correlate results obtained with the theory is made. Finally, efficiency measurements at microwave frequencies are described, including those made on 100 diodes fabricated for delivery at the conclusion of the contract.

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EVALUATION

The concept of the transfer of useful amounts of power via microwaves has been demonstrated. However, before practical systems are feasible the microwave rectification must be both highly efficient and reliable. Raytheon in their demonstration of the power transfer used a brute force approach to the rectification. Professor George of Purdue University measured the rectification efficiency of various solid state diodes and found the hot carrier device to be the most promising. Since no existing devices were capable of rectifying useful amounts of power, this effort was initiated to design and fabricate hot carrier devices and to perform circuit analysis as required to achieve maximum efficiency.

Motorola, after a slow start due to personnel changes, approached the task by carefully evaluating the various circuits used in rectification in order to isolate circuit and device losses. At the same time research was conducted on the basic device, its various parameters, and factors affecting the rectification. Part of the experimental work was at low frequencies where measurements were simpler and could be correlated with theory better. These results were then used for comparison with microwave measurements. The program provided the first thorough effort toward improving the rectification efficiency and isolating losses. The work will be valuable to any further development of the transfer of power via microwave concept. A side result is the general furtherance of hot carrier diodes as applied to detectors.

R. H. Chilton

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SECTION I

1.0 ANALYSIS OF IDEAL RECTIFIER CIRCUITS

1.1 INTRODUCTION

To understand the functioning of a microwave-to-dc converter, it is first necessary to understand how a low frequency converter behaves. This process may be divided into three parts. First, the simplest case is considered in which the frequency is sufficiently low that parasitic reactances may be ignored and the diodes in the circuit are considered perfect; i.e., they have zero forward voltage drop and resistance and an infinite reverse resistance.

Second, the effects of diode resistance, capacitance, lead inductance, etc. are considered. Finally, the wave aspects of the problem are considered; i.e., the effects that occur because of the finite size of the circuit with respect to the wavelength at the frequency of operation.

This section presents an analysis of the first part of this division and treats various rectifier circuits with various filtering schemes, considering the modes of operation and efficiencies achievable under ideal conditions.

Although this is an elementary problem, the results are highly important and in certain instances surprising. Above all, the analysis clearly points toward certain action which must be taken to achieve high efficiency operation in the microwave region.

1.2 FULL-WAVE BRIDGE CIRCUITS

1.2.1 Full-Wave Bridge Circuit Without Output Filter

The full-wave bridge circuit and associated waveforms are shown in Figure 1. Using the notation of this figure, the total power in the output circuit is given by

$$P_{out} = \frac{1}{2R_L}\left(\frac{E_P R_L}{R_G+R_L}\right)^2 = \frac{1}{2}\ \frac{E_P^2 R_L}{(R_G+R_L)^2} \qquad (1)$$

and this is a maximum for $R_L = R_G$. Thus

$$P_{out}\Big|_{max} = \frac{E_P^2}{8\ R_G}\ , \qquad (2)$$

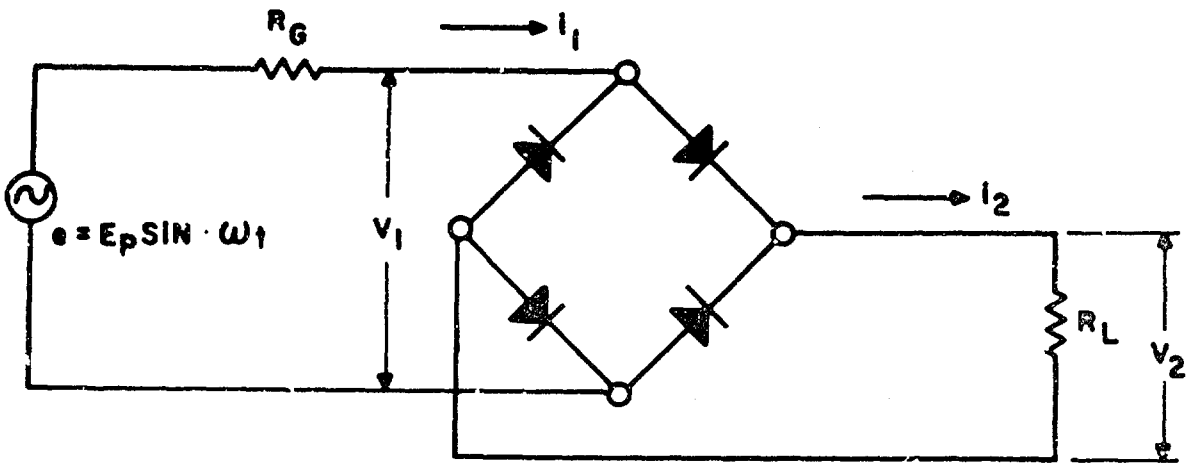
where E_P is the peak value of the input voltage.

Since this equals the maximum available power, P_A,

$$\eta = \frac{P_{out}\Big|_{max}}{P_A} = 100 \text{ percent.} \qquad (3)$$

However, if one considers only the dc power dissipation in the load

$$P_{out} = \frac{E_{DC}^2}{R_L} = \left(\frac{R_L}{R_G+R_L} \cdot \frac{2}{\pi} E_P\right)^2 \cdot \frac{1}{R_L} \qquad (4)$$



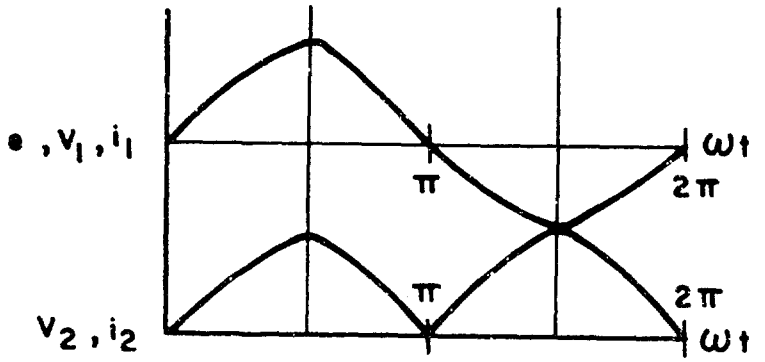


Figure 1. Full-Wave Bridge Circuit (Without Filter) and Associated Waveforms

and

$$P_{out}\Big|_{max} = \frac{E_P^2}{\pi^2 R_G} \tag{5}$$

where the factor $\frac{2}{\pi}$ is the dc term in the Fourier expansion of the output voltage waveform.

Hence

$$\eta = \frac{P_{out}\Big|_{max}}{P_A} = \frac{\frac{E_P^2}{\pi^2 R_G}}{\frac{E_P^2}{8R_G}} = \frac{8}{\pi^2} \tag{6}$$

or

$$\eta \cong 81 \text{ Percent} \tag{7}$$

Since a high frequency circuit without a filter would allow the second harmonic ripple term to radiate into space, 81 percent corresponds to the maximum possible efficiency under these conditions.

1.2.2 Full-Wave Bridge Circuit with Shunt Capacitor Output Filter

The circuit and associated waveforms are shown in Figure 2.

If it is assumed that C is large enough to provide negligible ripple voltage, then its impedance is very small compared to R_L.

From $\omega t = 0$ to $\omega t = \pi/2 - \phi$, the circuit appears open; from $\omega t = \pi/2 - \phi$ to $\omega t = \pi/2 + \phi$ it appears short circuited; etc.

From the waveforms

$$E_{DC} = E_P \sin (\pi/2 - \phi), \tag{8}$$

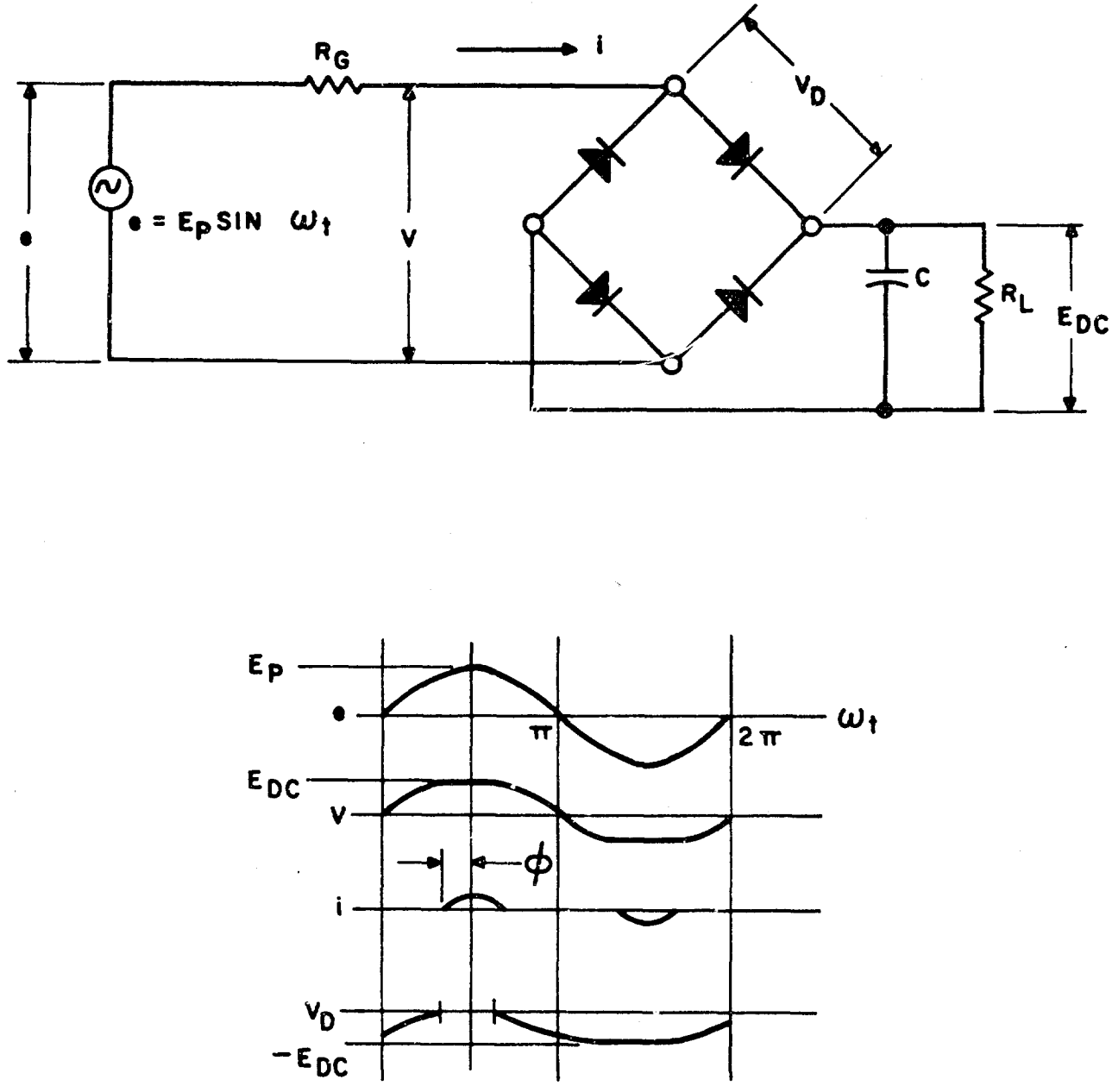


Figure 2. Full-Wave Bridge Circuit (Capacitor Output Filter) and Associated Waveforms

or

$$E_{DC} = E_P \cos \phi$$

Also

$$i = E_P \sin \omega t - E_{DC}, \ \pi/2 - \phi < \omega t < \pi/2 + \phi, \tag{9}$$

or

$$i = \frac{E_P}{R_G} (\sin \omega t - \cos \phi)$$

Thus, the charge flowing to the capacitor during the current pulse is

$$Q = \frac{1}{\omega} \int_{\pi/2-\phi}^{\pi/2+\phi} id(\omega t) = \frac{E_P}{\omega R_G} \int_{\pi/2-\phi}^{\pi/2+\phi} (\sin x - \cos \phi) dx \tag{10}$$

and upon evaluating the integral

$$Q = \frac{2E_P}{\omega R_G} (\sin \phi - \phi \cos \phi) \tag{11}$$

The charge flowing into R_L during a half-cycle is

$$Q' = \frac{1}{\omega} \int_0^{\pi} I_{DC} \, d(\omega t) = \frac{\pi E_{DC}}{\omega R_L} = \frac{\pi E_P}{\omega R_L} \cos \phi, \tag{12}$$

and since these two charges must be equal

$$\frac{2\,E_P}{\omega R_G}\,(\sin\phi - \phi\cos\phi) = \frac{\pi E_P}{\omega R_L}\cos\phi \qquad (13)$$

or

$$\frac{R_G}{R_L} = \frac{2}{\pi}\,(\tan\phi - \phi) \qquad (14)$$

The output power is

$$P_{out} = \frac{E_{DC}^2}{R_L} = \frac{E_P^2\cos^2\phi}{R_L}, \qquad (15)$$

and using equation 14 this becomes

$$P_{out} = \frac{2E_P^2\cos^2\phi\,(\tan\phi - \phi)}{\pi R_G} \qquad (16)$$

or

$$P_{out} = \frac{E_P^2}{\pi R_G}\,(\sin 2\phi - \phi[1 + \cos 2\phi]). \qquad (17)$$

To compute the efficiency for maximum output power, P_{out} must be maximized. A plot of P_{out} vs ϕ is given in Figure 3.

Hence, P_{out} is maximum for $\phi \cong \frac{3\pi}{8}$, and the efficiency is found from equation 17 to be

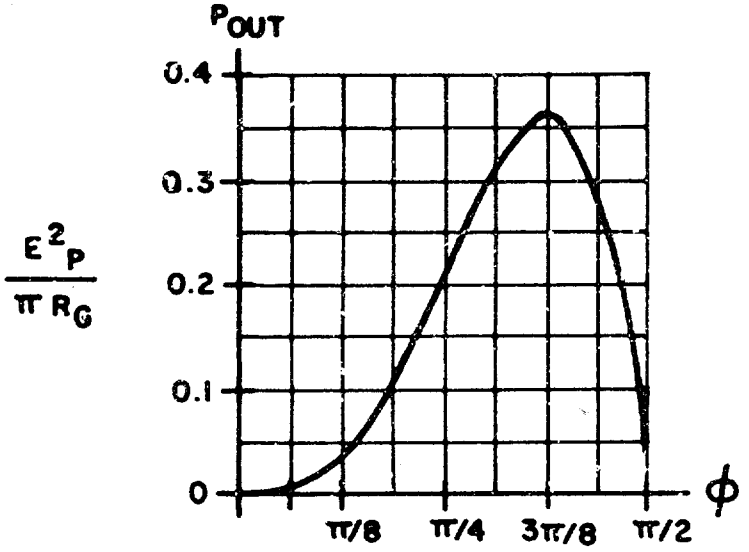


Figure 3. P_{out} vs ϕ for Full-Wave Bridge Circuit with Capacitor Output Filter

$$\eta = \frac{P_{out}}{P_A} = \frac{E_p^2/\pi R_G \ (\sin 2\phi - \phi \ [1+\cos 2\phi])}{E_p^2/8R_G} \qquad (18)$$

which for maximum output power is

$$\eta\Big|_{\phi = \frac{3\pi}{8}} \cong 0.362 \ \frac{8}{\pi} \cong 92 \text{ percent} \qquad (19)$$

It must be remembered that there are no losses in the circuit considered (perfect diodes), so the decrease in efficiency indicated by equation 19 is a fundamental limitation having to do with the existence of high-harmonic-content voltages and currents and not with any removable lossy elements.

1.2.3 Full-Wave Bridge Circuit with Series Choke Output Filter

The circuit and associated waveforms are shown in Figure 4.

The circuit parameters are the same as before except that here we assume that $X_L = \omega L >> R_L, R_G$, so that the output ripple is again small.

The operation of this circuit is somewhat more involved than the capacitor input circuit and is described below.

The inductance serves to maintain a constant current in the output circuit which must be alternately supplied by the two halves of the bridge. Due to the finite source resistance, this current causes a voltage drop, $I_{DC} R_G$, in the input circuit which causes the voltage supplied to the bridge to vanish prior to the input voltage, e.

At this time ($\omega t = \pi/2 + \phi$) the remaining two diodes begin to conduct, providing an additional current path for the output

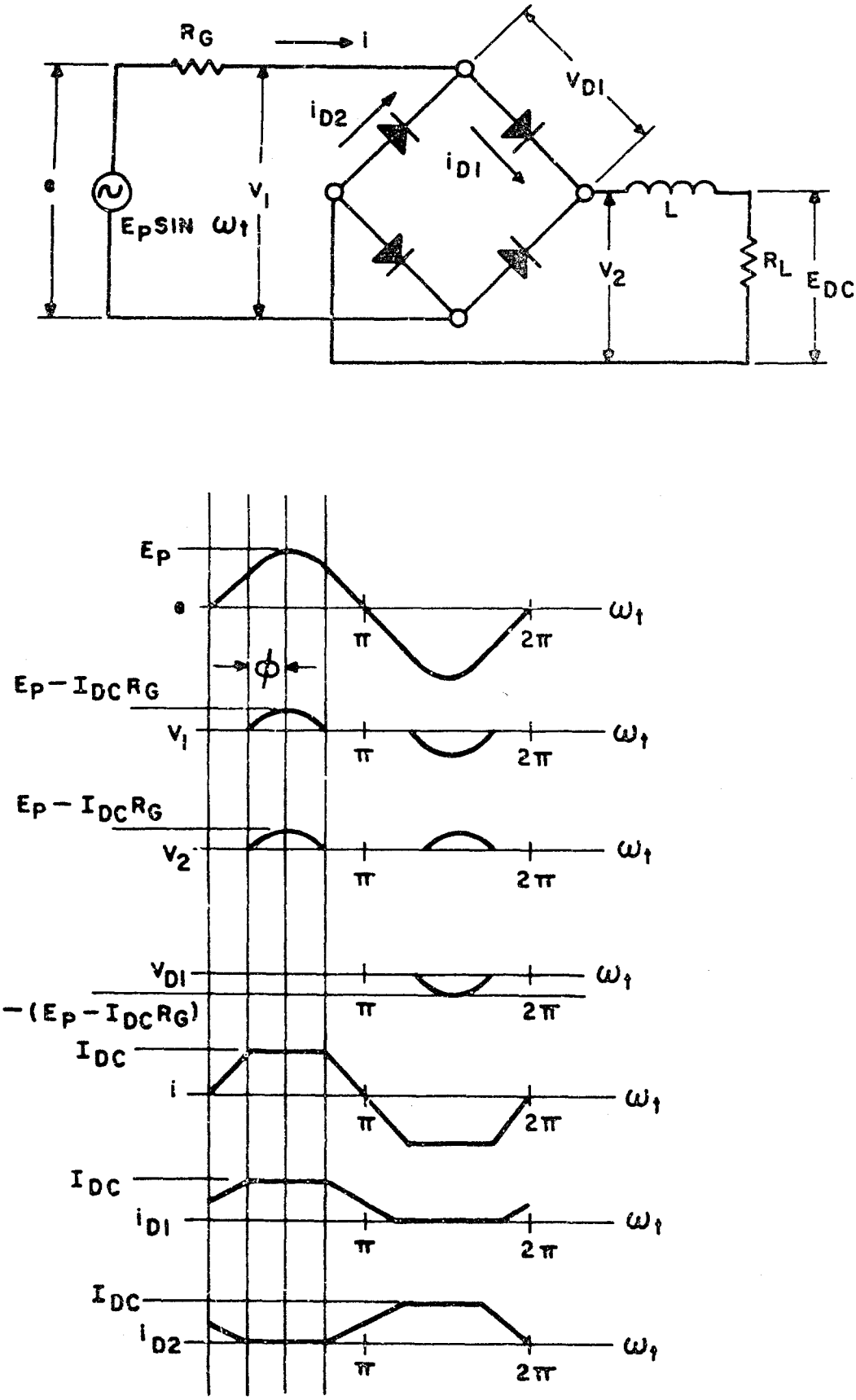


Figure 4. Full-Wave Bridge Circuit (Choke Output Filter) and Associated Waveforms

current. As the current through the first half of the bridge falls to zero with input voltage e, the current through the second half increases and maintains I_{DC} in the output. During this time, the voltage across the bridge remains at zero since $E_p \sin \omega t - i R_G = 0$ during this interval. At $\omega t = 3\pi/2 - \phi$, all of the output current is supplied by the second half of the bridge, the first half shuts off, and the voltage supplied to the bridge goes negative. This gives the relation

$$I_{DC} R_G = E_p \cos \phi \tag{20}$$

The dc output voltage is found by integrating voltage waveform v_2

$$E_{DC} = I_{DC} R_L = \frac{E_p}{\pi} \int_{\pi/2-\phi}^{\pi/2+\phi} (\sin x - \cos \phi) dx$$

$$= \frac{2E_p}{\pi} (\sin\phi - \phi \cos \phi). \tag{21}$$

Thus

$$I_{DC} R_L = \frac{E_p \cos\phi}{R_G} \cdot R_L = \frac{2E_p}{\pi} (\sin\phi - \phi \cos \phi) \tag{22}$$

and

$$\frac{R_L}{R_G} = \frac{2}{\pi} (\tan \phi - \phi) \tag{23}$$

For the output power

$$P_{out} = I_{DC}^2 R_L = \frac{E_p^2 \cos^2 \phi}{R_G^2} R_L$$

$$\frac{2E_p^2}{\pi R_G} \cos^2 \phi (\tan \phi - \phi)$$

$$= \frac{E_p^2}{\pi R_G} [\sin 2\phi - \phi(1+\cos 2\phi)] \qquad (24)$$

At this point we notice that there is an interesting duality between the capacitor output and the choke output filters. The input voltage and current waveforms are interchanged in going from one to the other and both filters provide the same phase-angle to resistance-ratio relation (equations 14 and 23) and output power relation (equations 17 and 24).

In view of the latter, the output power is again maximum for $\phi = \frac{3\pi}{8}$ and the efficiency in terms of the maximum available power is

$$\eta = \frac{P_{out}\Big|_{max}}{P_A} = 92 \text{ percent} \qquad (25)$$

Thus, shunting the ripple voltage and blocking it provide the same efficiency. Current and voltage are traded for one another in going from one scheme to the other. Also, the capacitor output filter makes the bridge operate in such a way that during the time interval $\omega t = 2\phi$, all four diodes are nonconducting (open circuit bridge) while the choke output filter results in all four diodes being in the conducting state (short circuit bridge) during the same interval.

1.2.4 Harmonic Analysis of Full-Wave Bridge Circuit with Filter

To gain further insight into the operation of the full-wave rectifier circuit with an output filter (capacitor or choke), the input waveforms will be Fourier analyzed and the power transfer and match provided at each harmonic calculated.

Thus, let

$$V(x) = \frac{V_o}{2} + \sum_n V_n \cos nx + \sum_m \overline{V}_m \sin mx \qquad (26)$$

where

$$V_n = \frac{1}{\pi} \int_0^{2\pi} V(x) \cos nx \, dx \qquad (27a)$$

$$\overline{V}_m = \frac{1}{\pi} \int_0^{2\pi} V(x) \sin mx \, dx, \qquad (27b)$$

and

$$i(x) = \frac{I_o}{2} + \sum_n I_n \cos nx + \sum_m \overline{I}_m \sin mx \qquad (28)$$

where

$$I_n = \frac{1}{\pi} \int_0^{2\pi} i(x) \cos nx \, dx \qquad (29a)$$

$$\overline{I}_m = \frac{1}{\pi} \int_0^{2\pi} i(x) \sin mx \, dx, \qquad (29b)$$

be the voltage and current input waveforms to the bridge. Since voltage and current are merely interchanged in going from capacitor

output filter to choke output filter, the capacitor filter will be considered to make the calculations specific.

In terms of the Fourier amplitude, the input power, which for perfect diodes equals the output power, may be expanded as follows

$$P_{in} = \frac{1}{2\pi} \int_0^{2\pi} i(x)V(x)dx = \frac{I_o V_o}{4} + \frac{1}{2} \sum_n I_n V_n + \frac{1}{2} \sum_m \bar{I}_m \bar{V}_m \qquad (30)$$

For the circuits under consideration, either sine terms or cosine terms of a given harmonic will be present, but not both; the current and voltage are either in phase or 180 degrees out of phase at each frequency. Thus, the input resistance at the k^{th} harmonic may be defined as

$$(R_{in})_k = \frac{V_k}{I_k} \qquad (31a)$$

or

$$(R_{in})_k = \frac{\bar{V}_k}{\bar{I}_k} \qquad (31b)$$

whichever applies. Since V_k and I_k (or $\bar{V}_k$ and $\bar{I}_k$) may be of opposite sign (180 degrees out of phase), $(R_{in})_k$ may be negative and the contribution to the power due to the k^{th} harmonic may also be negative, representing a loss due to reflection at that frequency.

For the full-wave circuits under consideration, there is no dc component in the input waveforms, and all of the waveforms are odd functions of x. Hence

$$I_o = V_o = V_k = I_k = o, \text{ for all } k, \tag{32}$$

or

$$i(x) = \sum_m \overline{I}_m \sin mx: \overline{I}_m = \frac{2}{\pi} \int_o^{\pi} i(x) \sin mx \, dx \tag{33}$$

$$V(x) = \sum_m \overline{V}_m \sin mx: \overline{V}_m = \frac{2}{\pi} \int_o^{2\pi} V(x) \sin mx \, dx \tag{34}$$

and

$$P_{in} = \frac{1}{2} \sum_m \overline{I}_m \overline{V}_m \text{ and } (R_{in})_k = \frac{\overline{V}_k}{\overline{I}_k} \tag{35}$$

Thus, for the capacitor output filter

$$\overline{I}_1 = \frac{2E_p}{\pi R_G} \int_{\pi/2-\phi}^{\pi/2+\phi} (\sin\chi - \cos\phi) \sin x \, dx$$

$$= \frac{E_p}{\pi R_G} (2\phi - \sin 2\phi) \tag{36}$$

and

$$\overline{V}_1 = \frac{2E_p}{\pi} \left[\int_o^{\pi/2-\phi} \sin^2 x \, dx + \cos\phi \int_{\pi/2-\phi}^{\pi/2+\phi} \sin x \, dx + \right.$$

$$\left. \int_{\pi/2+\phi}^{\pi} \sin^2 x \, dx \right] = \frac{E_p}{\pi} (\pi - 2\phi + \sin 2\phi) \tag{37}$$

This gives

$$(P_{in})_1 = \frac{1}{2}\bar{I}_1\bar{V}_1 = \frac{E_p^2}{2\pi^2 R_G}(2\phi - \sin 2\phi)(\pi - 2\phi + \sin 2\phi) \quad (38)$$

and

$$(R_{in})_1 = \frac{\bar{V}_1}{\bar{I}_1} = \frac{\pi - 2\phi + \sin 2\phi}{2\phi - \sin 2\phi} R_G. \quad (39)$$

For $\phi = \frac{3\pi}{8}$

$$(P_{in})_1 \Big|_{\phi = \frac{3\pi}{8}} = 0.125 \frac{E_p^2}{R_G} = \frac{E_p^2}{8R_G} \quad (40)$$

and

$$(R_{in})_1 \Big|_{\phi = \frac{3\pi}{8}} = 0.9\, R_G. \quad (41)$$

From this it is clear that there is a nearly perfect match at the fundamental frequency and that the efficiency would be 100 percent if no harmonics were present.

Without going through the calculations, one can see from the current and voltage waveforms that at the third harmonic, R_{in} is negative and that power is subtracted at the third harmonic. It is this term which results in most of the 8 percent loss calculated above (equation 25) and it appears in the form of a reflected wave which finally becomes absorbed in the source resistance, R_G.

Thus, high efficiency operation can be achieved only if some provision is made to prevent the third and higher harmonics from being absorbed in the source.

In view of these conclusions, which apply to the full-wave bridge circuit, it would appear worthwhile to carry through the same type of analysis for the half-wave, single diode circuit and this is done in the following subsection.

1.3 HALF-WAVE CIRCUITS

1.3.1 Half-Wave Circuit Without Output Filter

The circuit and associated waveforms are shown in Figure 5.

Here, the total output power is

$$P_{out} = \frac{1}{2\pi}\int_0^{2\pi} i(x)v(x)dx = \frac{E_p{}^2 R_L}{2\pi(R_L + R_G)^2}\int_0^{\pi} \sin^2 x\, dx = \frac{E_p{}^2 R_L}{4(R_L + R_G)^2} \tag{42}$$

and, hence, the efficiency is given by

$$\eta = \frac{2R_G R_L}{(R_L + R_G)^2} \tag{43}$$

which reaches a maximum of 50 percent for $R_L = R_G$.

However, if we consider only the dc component of the output power, we have from equation 30.

$$P_{DC} = \frac{I_o V_o}{4} \tag{44}$$

where:

$$I_o = \frac{1}{\pi}\int_0^{2\pi} i(x)dx = \frac{2E_p}{\pi(R_L + R_G)} \tag{45}$$

$$V_o = \frac{1}{\pi}\int_0^{2\pi} v(x)dx = \frac{2E_p R_L}{\pi(R_L + R_G)} \tag{46}$$

so,

$$P_{DC} = \frac{E_p{}^2 R_L}{\pi^2(R_L + R_G)^2} \tag{47}$$

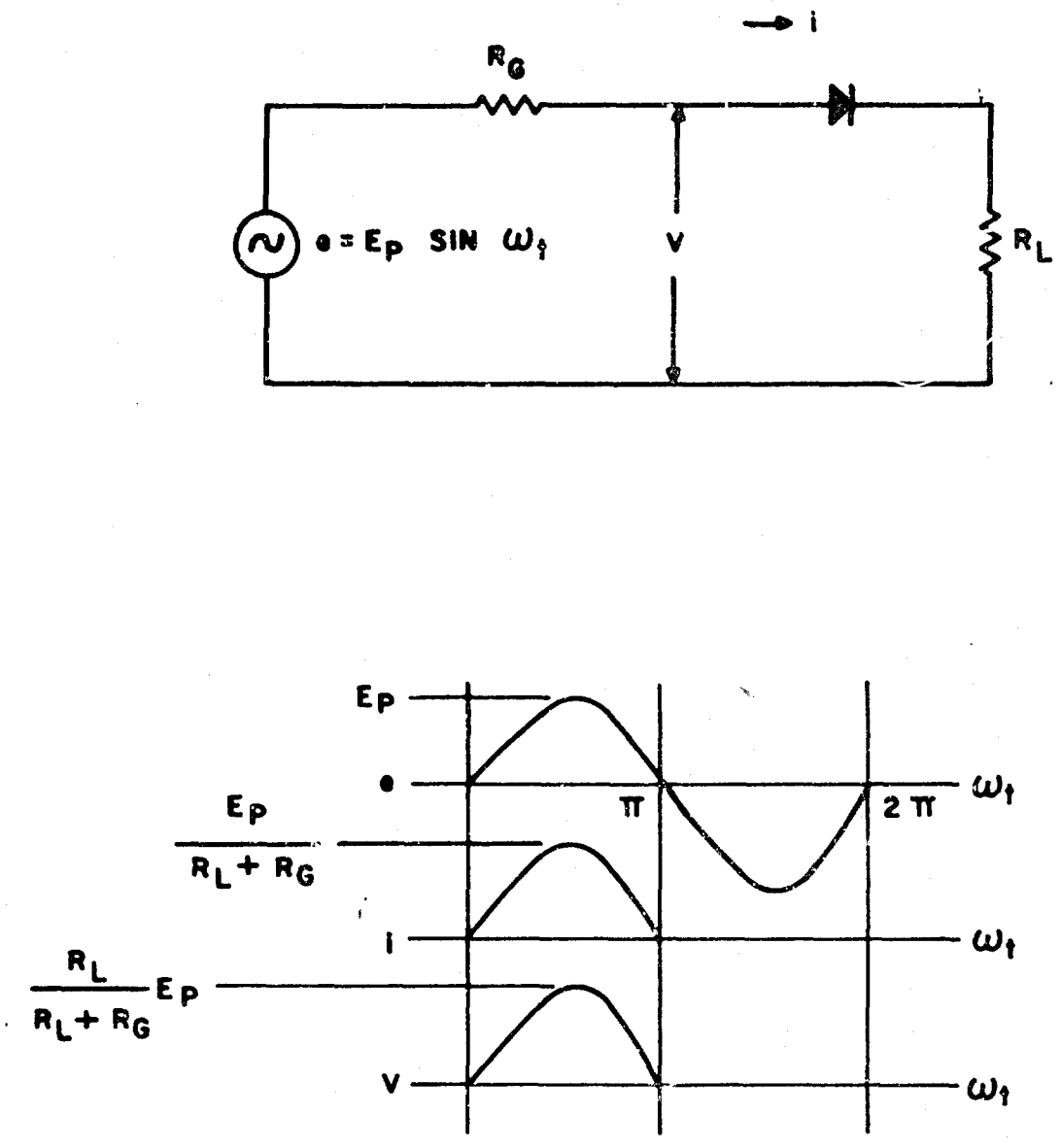


Figure 5. Half-Wave Circuit (Without Filter) and Associated Waveforms

and

$$\eta\Big|_{max} = \frac{2}{\pi^2} \cong 20.3\% \text{ for } R_L = R_G \tag{48}$$

1.3.2 Half-Wave Circuit with Shunt Capacitor Output Filter

The circuit and associated waveforms are shown in Figure 6, where we again assume C large.

As in the full-wave bridge circuit

$$E_{DC} = E_p \cos \phi \tag{49}$$

$$i = \frac{E_p \sin wt - E_{DC}}{R_G}: \quad \pi/2 - \phi < \omega t < \pi/2 + \phi . \tag{50}$$

The charge flowing during the current pulse is the same as before

$$Q = \frac{2E_p}{\omega R_G} (\sin \phi - \phi \cos \phi), \tag{51}$$

but the charge flowing into R_L during the entire cycle is twice that for the bridge circuit, or

$$Q' = \frac{2\pi E_p}{\omega R_L} \cos \phi \tag{52}$$

so

$$\frac{2\pi E_p \cos\phi}{\omega R_L} = \frac{2E_p}{\omega R_G} (\sin\phi - \phi \cos \phi) \tag{53}$$

or

$$\frac{R_G}{R_L} = \frac{1}{\pi} (\tan \phi - \phi). \tag{54}$$

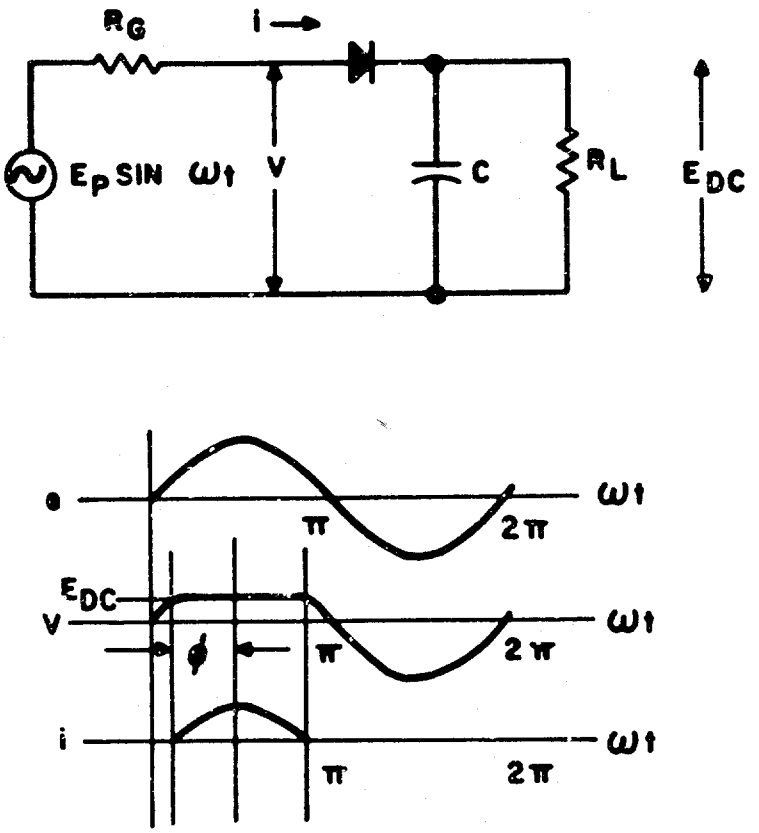


Figure 6. Half-Wave Circuit (with Capacitor Output Filter) and Associated Waveforms

Thus, the output power becomes

$$P_{out} = \frac{E_{DC}^2}{R_L} = \frac{E_p^2 \cos^2\phi}{R_L} = \frac{E_p^2 \cos^2\phi (\tan\phi - \phi)}{\pi R_G} \tag{55}$$

or

$$P_{out} = \frac{E_p^2}{2\pi R_G} (\sin 2\phi - \phi [1 + \cos 2\phi]) \tag{56}$$

As before, this is maximized for $\phi = \frac{3\pi}{8}$, but now the maximum output power is

$$P_{out}\Big|_{max} = 0.326 \frac{E_p^2}{2\pi R_G} = 0.163 \frac{E_p^2}{\pi R_G} \tag{57}$$

and

$$\eta\Big|_{\phi = \frac{3\pi}{8}} = 46 \text{ percent.} \tag{58}$$

1.3.3 Harmonic Analysis of Half-Wave Circuit with Filter

From equations 26 through 29

$$V_o = \frac{E_p}{\pi} \left[2 \int_o^{\pi/2-\phi} \sin x dx + \cos\phi \int_{\pi/2-\phi}^{\pi/2+\phi} dx - \int_o^{\pi} \sin x dx \right]$$

$$= \frac{E_p}{\pi} \left[2(-\cos x) \Big|_o^{\pi/2-\phi} + \cos\phi \, (2\phi) + \cos\phi \Big|_o^{\pi} \right]$$

$$= \frac{2E_p}{\pi} [\phi \cos\phi - \sin\phi]. \tag{59}$$

Thus

$$V_o\Big|_{\phi = \frac{3\pi}{8}} = -\ 0.300\ E_p, \tag{60}$$

so

$$V_{DC} = \frac{V_c}{2} = -0.150\ E_p. \tag{61}$$

For I_o,

$$I_o = \frac{E_p}{\pi R_G} \left[\int_{\pi/2-\phi}^{\pi/2+\phi} (\sin x - \cos\phi)\, dx \right]$$

which simplifies to

$$I_o = \frac{2E_p}{R_G} (\sin\phi - \phi \cos\phi). \tag{62}$$

Thus,

$$I_{DC} = I_o\Big|_{\phi = \frac{3\pi}{8}} = 0.\frac{150}{R_G} E_p. \tag{63}$$

Here, $V_1 = o$ and

$$\overline{V}_1 = \frac{E_p}{\pi} \left[2 \int_c^{\pi/2-\phi} \sin^2 x dx + \cos\phi \int_{\pi/2-\phi}^{\pi/2+\phi} \sin x dx + \int_o^{\pi} \sin^2 x dx \right].$$

$$\therefore\ \overline{V}_1 = \frac{E_p}{\pi} [\pi - \phi + \tfrac{1}{2} \sin 2\phi], \tag{64}$$

and

$$\bar{V}_1\Big|_{\phi = \frac{3\pi}{8}} = \frac{E_p}{\pi}\left(3.14 - 1.118 + \frac{0.707}{2}\right) = 0.735\, E_p. \quad (65)$$

Similarly, $I_1 = o$ and

$$\bar{I}_1 = \frac{E_p}{\pi R_G}\left[\int_{\pi/2-\phi}^{\pi/2+\phi} (\sin x - \cos\phi)\sin x\,dx\right]$$

$$= \frac{E_p}{\pi R_G}\left[\int_{\pi/2-\phi}^{\pi/2+\phi} \sin^2 x\,dx - \int_{\pi/2-\phi}^{\pi/2+\phi} \cos\phi \sin x\,dx\right]$$

$$= \frac{E_p}{\pi R_G}\left[\phi - \frac{\sin 2\phi}{2}\right], \quad (66)$$

so

$$\bar{I}_1\Big|_{\phi = \frac{3\pi}{8}} = \frac{E_p}{\pi R_G}\left(1.18 - \frac{0.707}{2}\right)$$

(67)

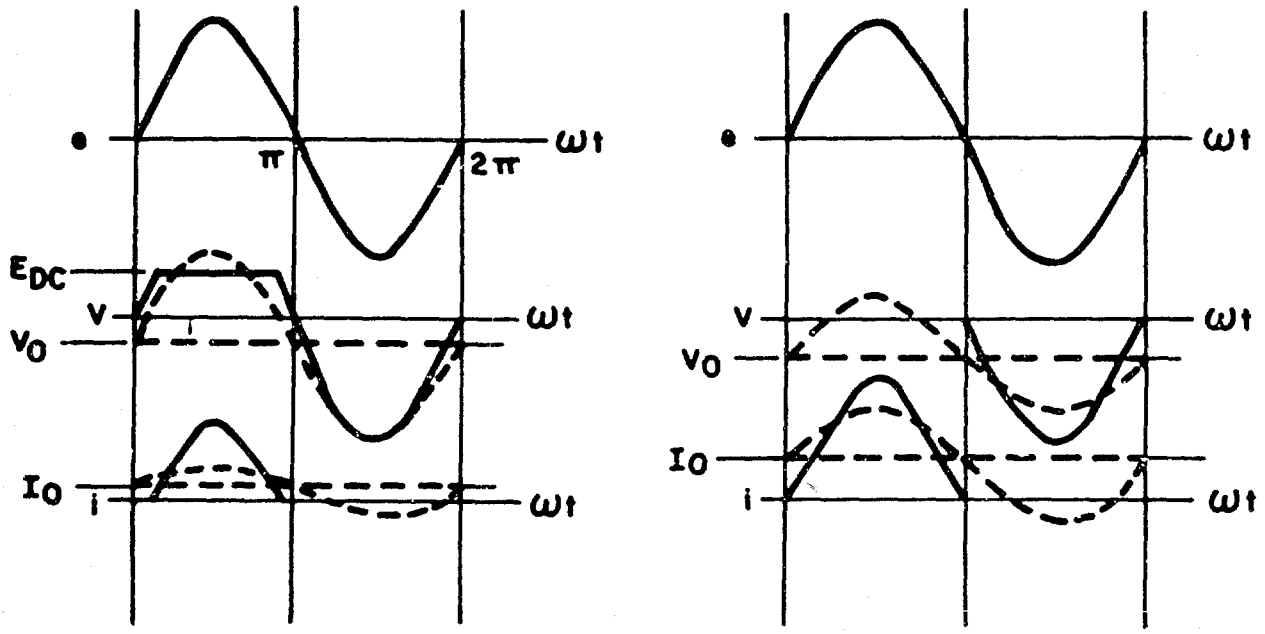
$$\bar{I}_1\Big|_{\phi = \frac{3\pi}{8}} = 0.263\, \frac{E_p}{R_G}.$$

Notice that there is a major difference between the full-wave circuits and the half-wave circuit. In the former it was possible to present a perfect match at the fundamental frequency so that only harmonics were reflected, whereas from equations 64 and 66 it is seen that

$$(R_{in})_1 = \frac{\overline{V}_1}{\overline{I}_1} = \frac{\pi - \phi + \frac{1}{2}\sin 2\phi}{\phi - \frac{1}{2}\sin 2\phi} R_G \qquad (68)$$

and the coefficient of R_G in this expression becomes unity only in the limiting case of $\phi \to \pi/2$ for which R_L and $E_{DC} \to 0$, as seen from equations 54 and 49. Thus, there is always a reflection at the fundamental frequency.

This is shown in Figure 7 where the waveforms and their dc and fundamental components are sketched.



Normal Operation Resulting in Mismatch at Fundamental Frequency

Limiting Case of Zero Output Voltage Resulting in Match at Fundamental Frequency

Figure 7. Waveforms Showing Mismatch and Match at Fundamental Frequency for Half-Wave Circuit with Capacitor Output Filter

1.4 INPUT FILTERING

1.4.1 Introduction

In the previous sections, it was demonstrated that none of the rectifier circuits considered is capable of achieving 100 percent efficiency, even with lossless diodes, due to the generation of harmonic currents and voltages by the diodes and the subsequent absorption of these components by the source resistance, R_G.

The efficiencies calculated run from 20.3 percent for the unfiltered half-wave circuit to 92 percent for the filtered full-wave circuit.

This situation naturally prompts one to inquire as to whether some suitable form of filtering at the input to the diode(s) can prevent this absoprtion from taking place and thus increase the efficiency theoretically achievable. The following sections are devoted to this question where the circuits treated previously are again considered.

1.4.2 Input Filtering with Full-Wave Rectifiers

Since we are interested in preventing third and higher harmonics from reaching the source from the diode, we have the option of interposing between source and rectifier a filter which serves as a short circuit from input to output at the fundamental frequency and either open circuits, or short circuits the harmonics to ground.

An example of the former is shown in Figure 8a and of the latter in Figure 8b. In each case, the circuits are tuned to the fundamental frequency and are assumed to be of very high Q.

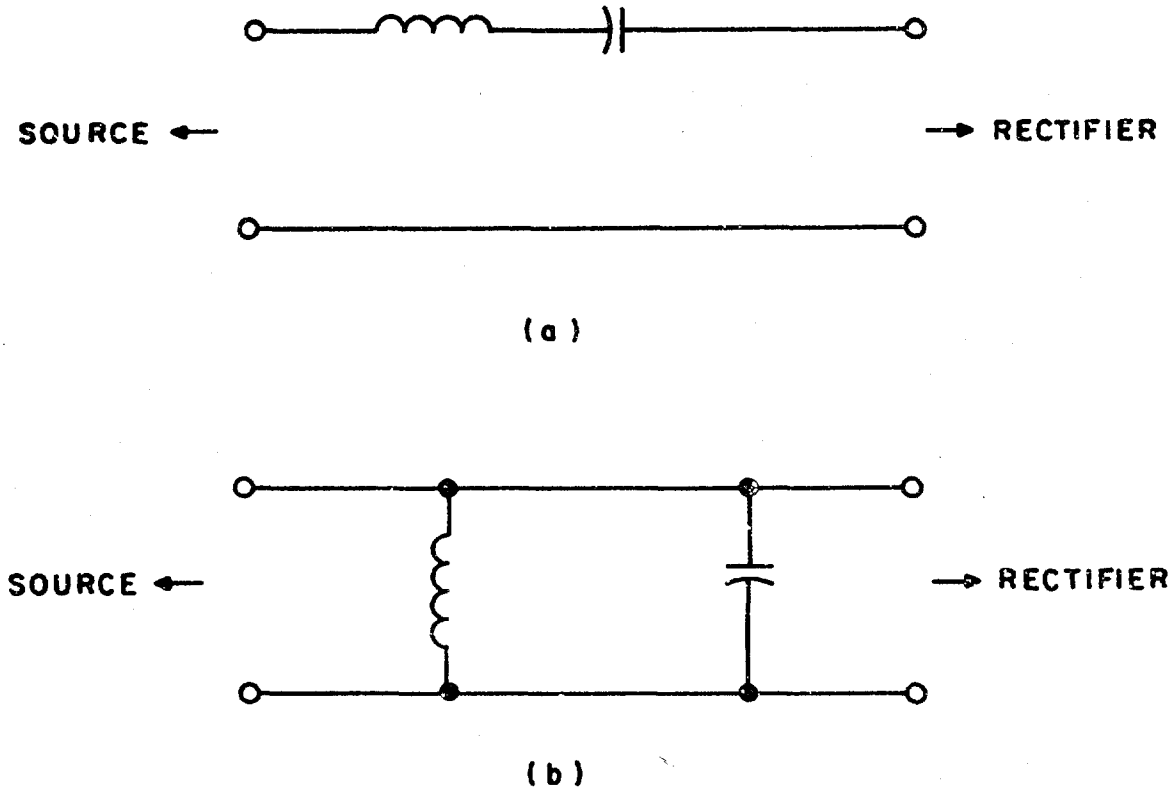


Figure 8. Examples of Input Circuit Filters
(a) Open Circuit to Harmonics
(b) Short Circuit to Harmonics

One can gain a qualitative understanding of the effect of these filters on the circuits of Figure 2 and Figure 4, i.e., the full-wave bridge with shunt capacitor and series choke output filter respectively, by referring to the waveforms for these circuits without input filtering and keeping in mind that the two are duals of one another.

Thus, the series resonant filter of Figure 8a when used with the capacitor output circuit forces the input current, i, of Figure 2, to be purely fundamental with the result that the input voltage approximates a square wave of amplitude, E_{DC}. The dual of

this situation is the parallel tuned circuit of Figure 8b, used on the input of the choke output circuit of Figure 4, resulting in a square wave current of amplitude I_{DC}.

The alternate possibilities consist of the use of the shunt tuned input filter with the capacitor output circuit, and the series tuned filter with the choke output circuit. In the former instance, the input voltage is pure fundamental and the input current approximates a Dirac delta function which, when integrated, yields the total charge flowing in the dc circuit per half cycle.

Similarly, in the latter case, the input current is pure fundamental which results in a delta function input voltage waveform.

These four situations are summarized in Figure 9 where the schematic diagrams and waveforms are shown. It is to be noted that in each instance both the current and voltage appearing at the input terminals to the entire circuit, i.e., at the input filter, are pure fundamental and that a perfect match may be achieved by choosing R_L properly.

Thus, for the circuit of Figure 9a, a match is secured when the peak value of the input current is

$$I'_p = \frac{E_p}{2R_G}. \tag{69}$$

and the peak input voltage

$$E'_p = \frac{E_p}{2} \tag{70}$$

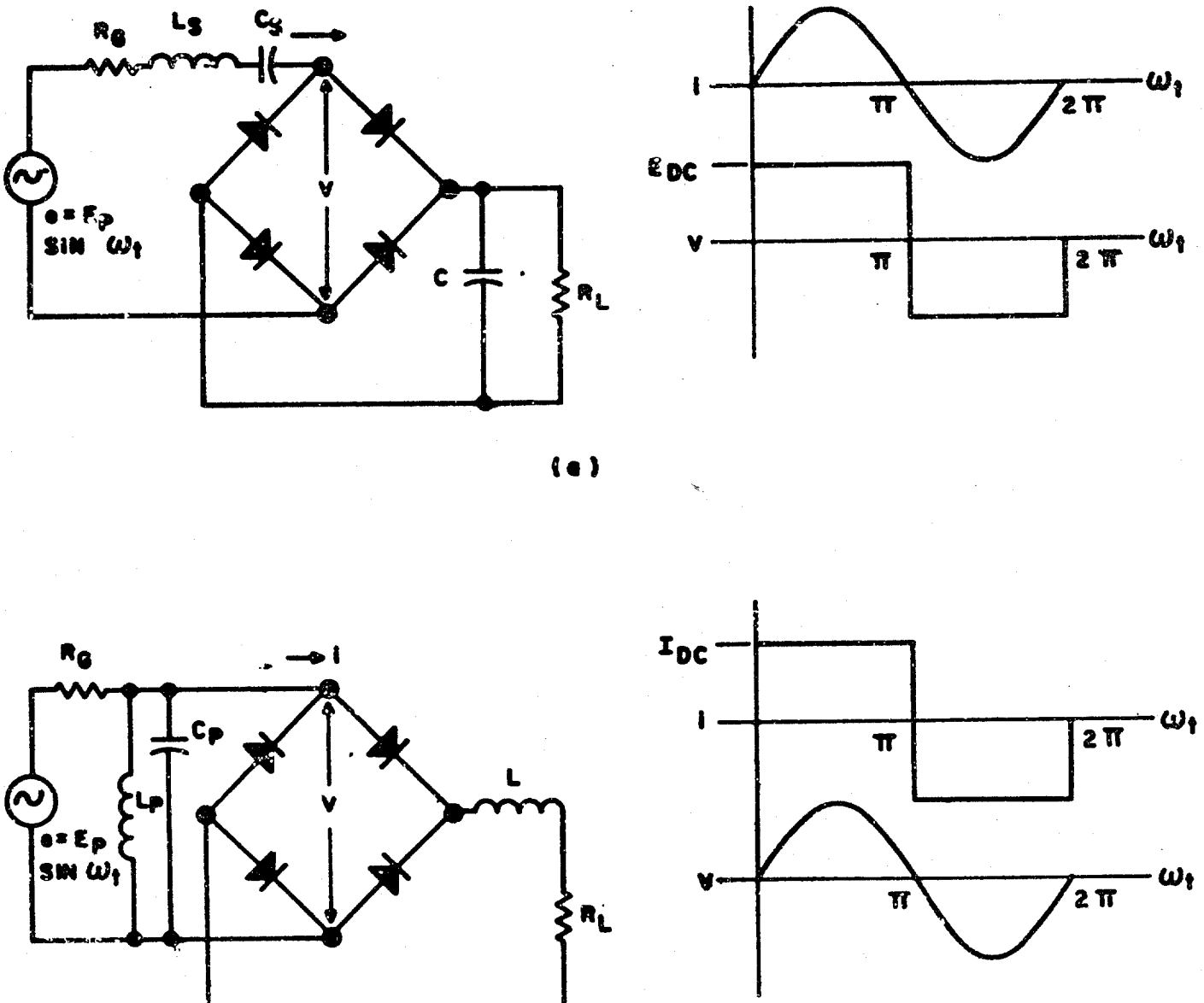
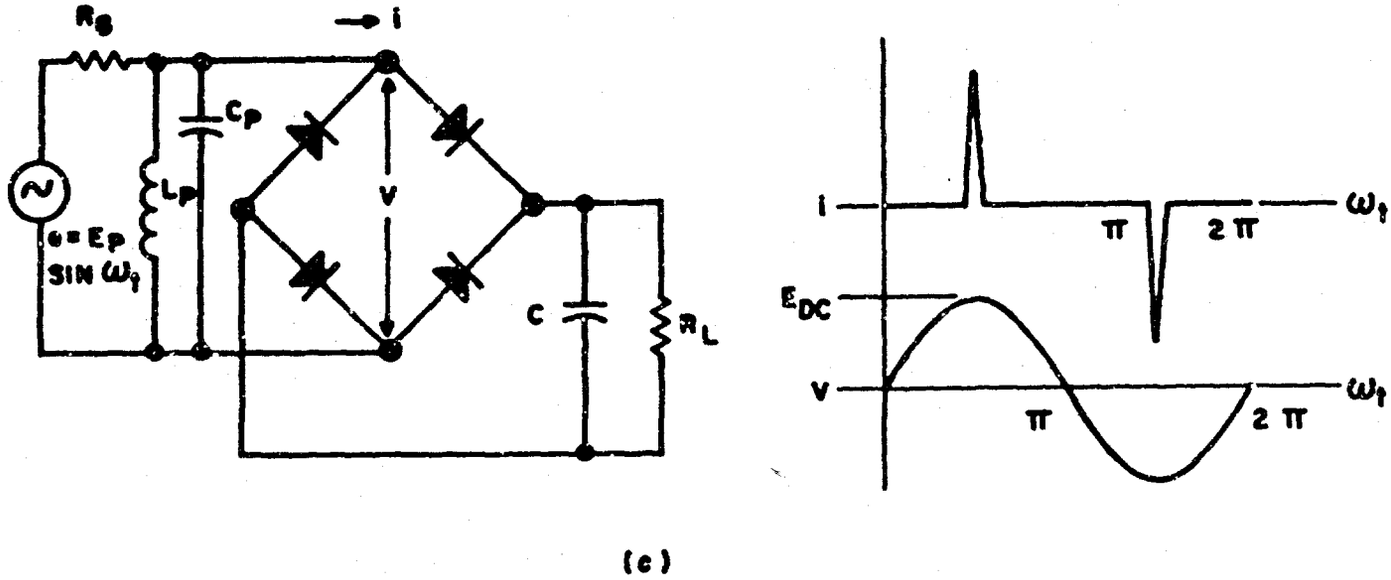
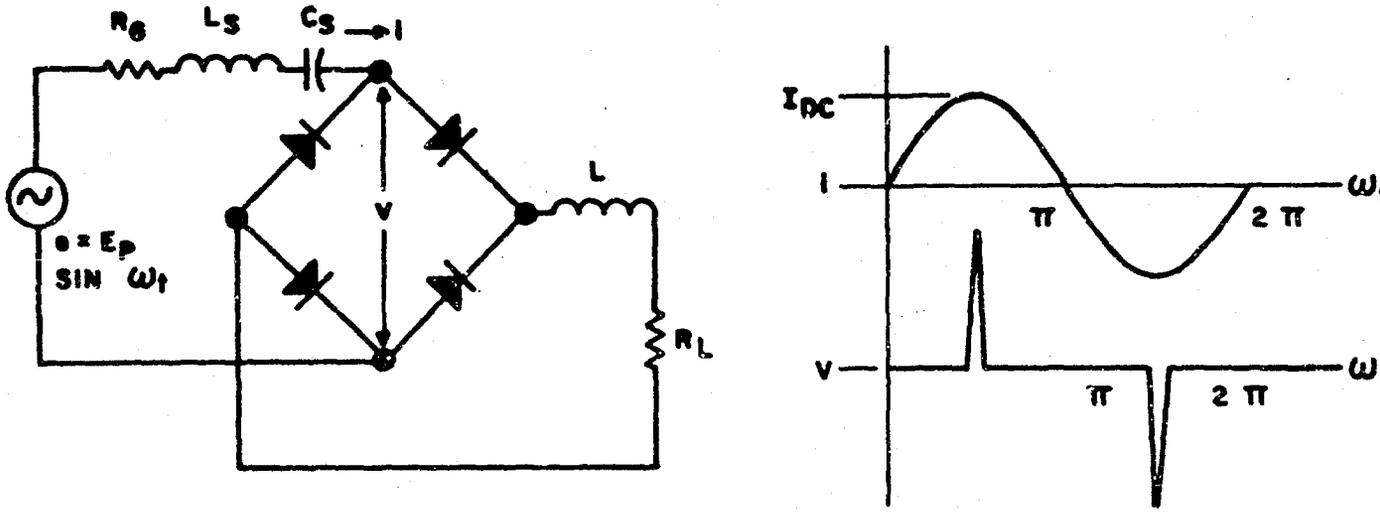


Figure 9. Summary of Combinations of Input and Output Filtering Schemes for the Full-Wave Bridge Rectifier



(c)



(d)

Figure 9. (cont'd.) Summary of Combinations of Input and Output Filtering Schemes for the Full-Wave Bridge Rectifier

This is just the fundamental component of the square wave voltage, v, whose peak value is E_{DC}, so

$$\frac{E_p}{2} = \frac{4}{\pi} \cdot E_{DC} \tag{71}$$

The current waveform for the output current is full-wave, as shown in Figure 1, so that the dc output current is

$$I_{DC} = \frac{E_{DC}}{R_L} = \frac{2}{\pi} I'_p = \frac{E_p}{\pi R_G} \tag{72}$$

From (71) and (72) we have

$$\boxed{R_L = \frac{\pi^2}{8} R_G} \tag{73}$$

as the condition for match.

From (71) and (73) we see that the output power is

$$P_o\Big|_{max} = \frac{E_{DC}^2}{R_L} = \frac{E_p^2}{8R_G} \tag{74}$$

which is also the maximum available power. Thus, 100 percent efficiency is achieved.

A similar analysis for the circuit of Figure 9b yields the relation

$$\boxed{R_L = \frac{8}{\pi^2} R_G} \tag{75}$$

corresponding to (73) above, and again 100 percent efficiency is achieved.

Likewise, for the circuit of Figure 9c,

$$E_{DC} = \frac{E_p}{2} \tag{76}$$

and a match is secured for

$$\boxed{R_L = 2R_G} \tag{77}$$

while for that of Figure 9d,

$$I_{DC} = \frac{E_p}{2R_G} \tag{78}$$

and,

$$\boxed{R_L = \frac{R_G}{2}} \tag{79}$$

Once again, we see the duality expressed in the reciprocal relationships for R_L.

A point worth mentioning is that for cases (a) and (b) of Figure 9, conduction of the diodes occurs throughout the cycle so that effectively C and R_L in (a) and L and R_L in (b) appear in series and in parallel respectively, with the input filter. This alters the tuning, but since the conditions for good harmonic rejection by the filters are

$$\frac{1}{\omega C_s} >> R_G \tag{80}$$

and

$$\omega L_p << R_G \tag{81}$$

for the two cases, whereas the requirements for low output ripple are

$$\frac{1}{\omega C} << R_L \tag{82}$$

and

$$\omega L >> R_L \tag{83}$$

we see that the effect is small in each case.

1.4.3 Input Filtering with the Half-Wave Rectifier

As was pointed out in Section 1.3.3, the half-wave circuit differs from the full-wave in that in addition to the harmonic reflection, there is also always a reflection at the fundamental frequency as well. Thus, it might be thought that no suitable filtering can be found for this circuit.

However, a closer look at the harmonic analysis shows that the basic problem is a reflected dc component and that when this is eliminated, a match at the fundamental can be secured.

To see this we consider the circuit of Figure 10a which now includes an RF choke at the input of the diode acting as a filter to prevent a dc voltage from appearing at this point.

We proceed in the efficiency calculations as in the past. For the output voltage we now have

$$E_{DC} = V_{DC} + E_p \cos \phi \tag{84}$$

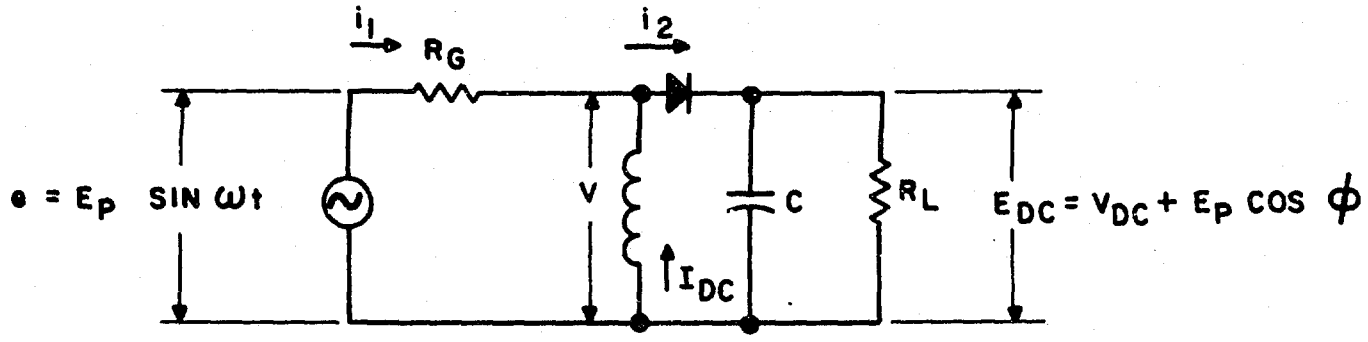


Figure 10(a). Half-Wave Rectifier Circuit with RF Choke

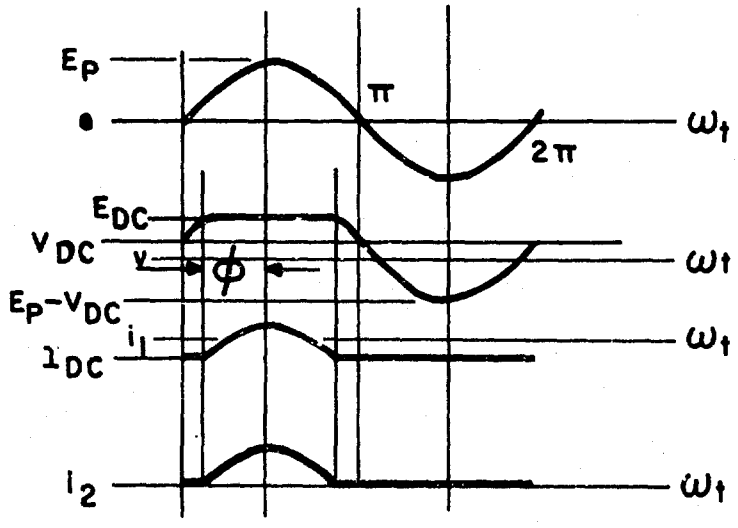


Figure 10(b). Waveforms Associated with Half-Wave Rectifier Circuit with RF Choke

where

$$V_{DC} = \frac{V_o}{2} = \text{dc component of clipped voltage waveform.}$$

The current flowing through the diode, i_2, is the same as before,

$$i_2 = \frac{E_p \sin \omega t - E_{DC}}{R_G}, \quad \pi/2 - \phi < \omega t < \pi/2 + \phi \tag{85}$$

which is equation 50. Hence, the charge transferred during this current pulse is also the same,

$$Q = \frac{2E_p}{R_G} (\sin \phi - \phi \cos \phi) \tag{86}$$

However, the charge flowing through R_L each cycle is now

$$Q' = \frac{2\pi E_{DC}}{R_L} = \frac{2\pi}{R_L} \left(\frac{V_o}{2} + E_p \cos \phi\right). \tag{87}$$

Thus, we obtain,

$$\frac{R_G}{R_L} = \frac{E_p}{\pi} \frac{\sin \phi - \phi \cos \phi}{\frac{V_o}{2} + E_p \cos \phi} \tag{88}$$

upon setting $Q = Q'$.

The output power is thus

$$P_{out} = \frac{(E_{DC})^2}{R_L} = \left(\frac{V_o}{2} + E_p \cos \phi\right) (\sin \phi - \phi \cos \phi) \frac{E_p}{\pi R_G}. \tag{89}$$

From equation 59 we have

$$V_o = \frac{2E_p}{\pi} (\sin \phi - \phi \cos \phi) \tag{90}$$

and substituting this into the above, we obtain

$$P_{out} = \frac{E_p^2}{\pi R_G} [\frac{1}{\pi} (\sin \phi - \phi \cos \phi) + \cos \phi] [\sin \phi - \phi \cos \phi] \tag{91}$$

where it is to be noted that we have defined V_o as a positive quantity in this instance.

It can be seen that this expression is a maximum for $\phi = \frac{\pi}{2}$,

$$P_{out}\Big|_{\phi = \frac{\pi}{2}} = \frac{Ep^2}{\pi^2 R_G} \tag{92}$$

so that,

$$\eta\Big|_{\phi = \frac{\pi}{2}} = \frac{8}{\pi^2} = 81\%. \tag{93}$$

If we now calculate the match at the fundamental frequency we obtain the same result as equation 68,

$$(R_{in})_1 = \frac{\overline{V}_1}{I_1} = \frac{\pi - \phi + \frac{1}{2} \sin 2\phi}{\phi - \frac{1}{2} \sin 2\phi} R_G \tag{94}$$

but now we have $\phi = \frac{\pi}{2}$ as the case of maximum power rather than zero output so that,

$$(R_{in})_1\Big|_{\phi = \frac{\pi}{2}} = R_G \tag{95}$$

or

$$R_L\Big|_{\phi = \frac{\pi}{2}} = R_G \ , \tag{96}$$

thus showing that a perfect match may be achieved at the fundamental.

Next, we consider the effect of the filters of Figure 8 on the half-wave circuit of Figure 10. The two resulting circuits, with their attendant waveforms, are shown in Figure 11.

From an analysis identical with that carried out for the full-wave circuits we find that for the series input filter,

$$R_L = \frac{R_G}{2} \tag{97}$$

and for the shunt filter,

$$R_L = 2R_G \tag{98}$$

for a perfect match and corresponding 100 percent efficiency.

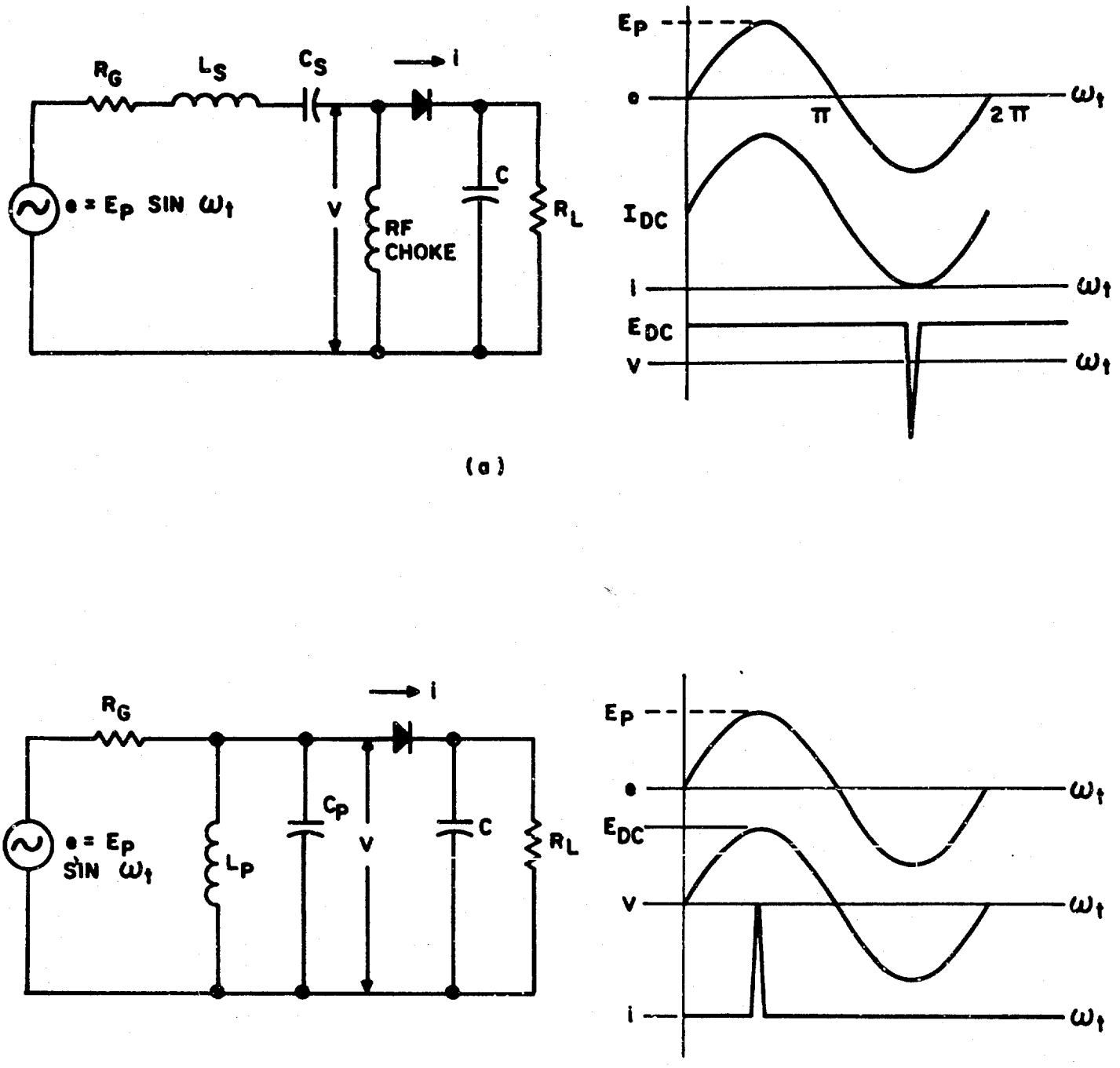


Figure 11. Half-Wave Rectifier with Series and Shunt Input Filtering

1.5 DISCUSSION OF RESULTS OF ANALYSIS

The foregoing analysis has demonstrated that while the usual full-wave and half-wave rectifier circuits are incapable of providing 100 percent conversion efficiency, they may be made to do so by the introduction of suitable filtering at the input to the rectifier.

Although all of the cases treated do yield 100 percent theoretical efficiency, they are not all equivalent in performance from a practical standpoint. This can be seen at a glance by examination of the waveforms generated by each circuit. Clearly, delta function currents and voltages pose problems of burnout and breakdown and such operation must be avoided. Also, even without considering the delta function voltage cases, it can be seen that the reverse voltage seen by each diode varies from circuit to circuit, so that the device design, and ultimately the efficiency, will be different for the various circuits when losses are taken into account.

In the next section of this report, we examine the effects which nonideal diode characteristics and other lossy elements have on the operation and overall efficiency of the circuits treated above.

SECTION II

2.0 ANALYSIS OF LOSSES

2.1 INTRODUCTION

In this section we begin by looking at the equivalent circuit for the hot carrier diode, and from this we attempt an approximate analysis of the losses to be expected in the various circuits discussed in Section 1.0. Also, the effect of the finite Q of the resonant circuits is considered.

2.2 EQUIVALENT CIRCUIT FOR DIODE

An understanding of the significant diode parameters can be gained by referring to Figure 12 which shows a schematic representation of the equivalent circuit of a single hot carrier diode. The individual elements shown in this circuit can be related to the actual device by comparison with Figure 13, which is a scale drawing of one of Motorola's typical diodes.

Thus, the active part of the diode, i.e., the barrier region, is represented by a shunt combination of a voltage dependent capacitance, C_b, and a voltage dependent resistance, shown as an ideal diode* in series with a resistor, R_b. In series with this combination is a resistance, r_s, which is frequency dependent as well as voltage dependent. This resistance consists of several parts and includes a spreading resistance in the heavily doped substrate, a series resistance due to more lightly doped material in the epitaxial layer but outside the barrier region, lead resistance and possible contact resistances due to wire bonds, etc.

*An ideal diode in this context is a nonlinear resistor obeying the diode equation: $I = I_s \left[\exp\left(\frac{qv}{kT}\right) - 1\right]$.

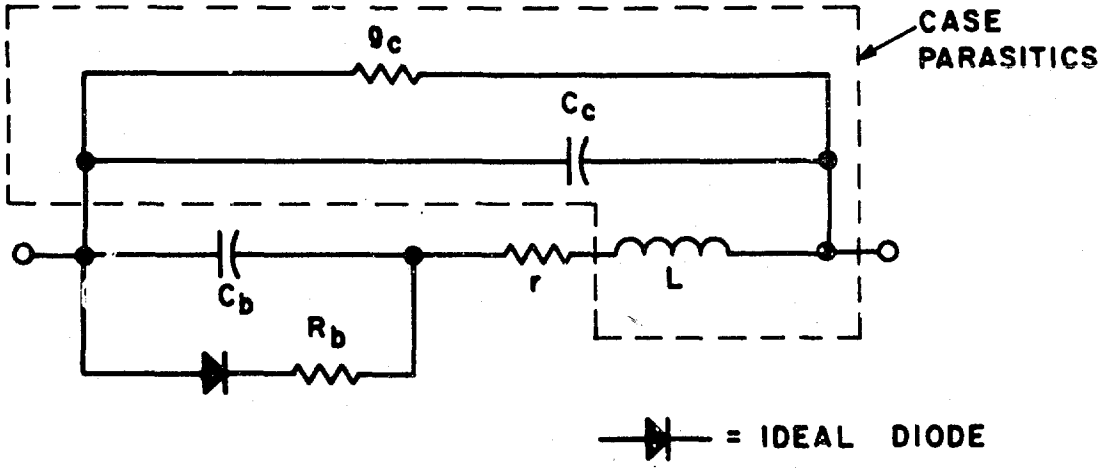


Figure 12. Equivalent Circuit of a Single Hot Carrier Diode

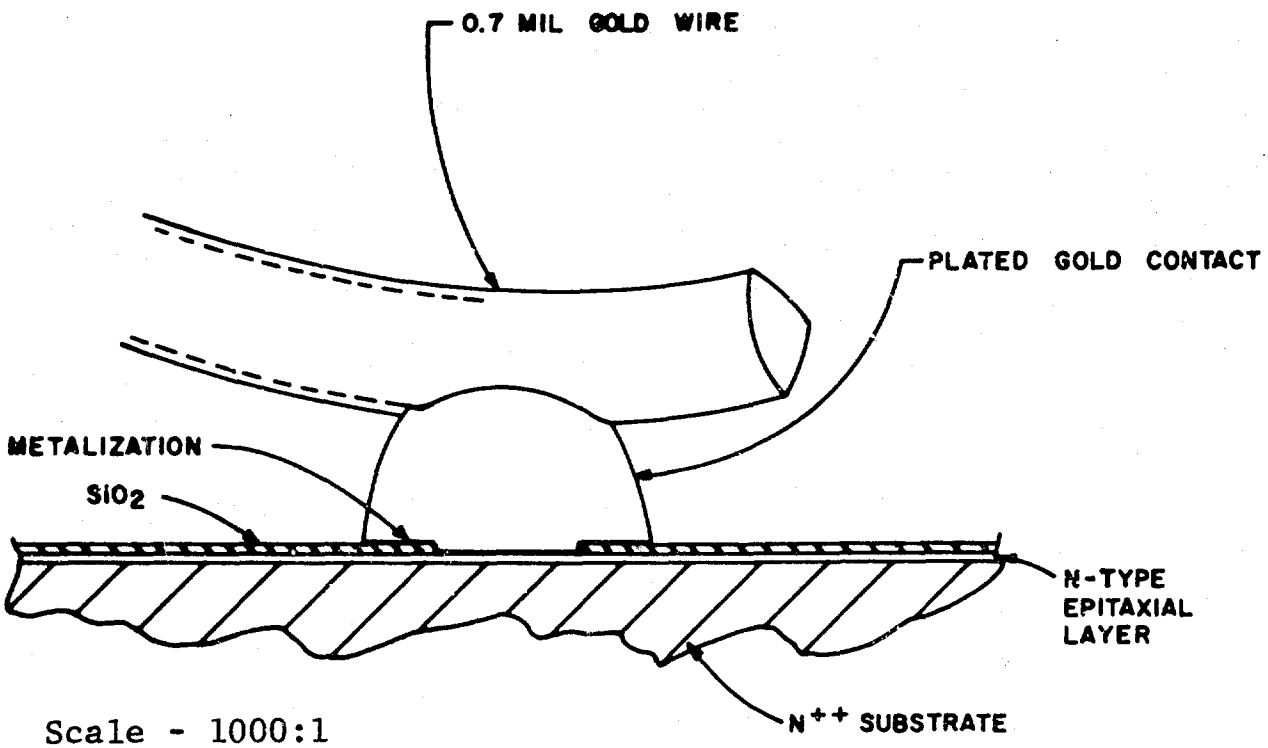


Figure 13. Hot Carrier Diode Physical Arrangement

In addition to providing a certain amount of resistance, the lead wire (or wires) also introduces a series inductance, L. Shunting this entire circuit is a case capacitance, C_c, and case conductance, g_c, the latter being due to the dielectric loss of the case ceramic material.

Considering the above equivalent circuit, a series of measurements on individual diodes can be performed, and the parameters so obtained related to various elements of the circuit. A description of these measurements is given in a later section.

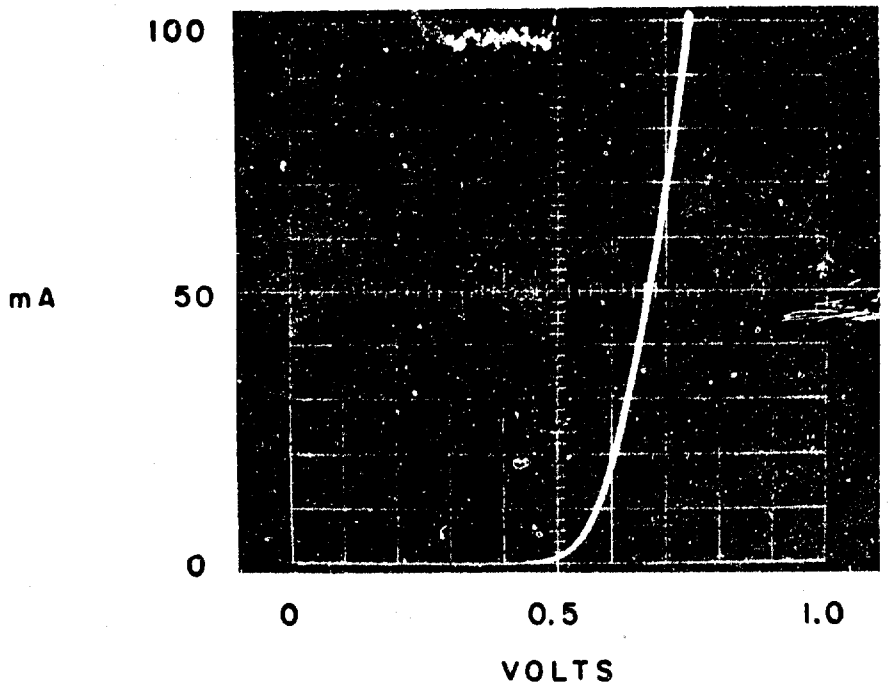
For the present we merely list in tabular form some typical values for the above parameters so that the relative importance of each may be judged.

TABLE I

TYPICAL VALUES OF HOT CARRIER DIODE EQUIVALENT CIRCUIT PARAMETERS

Parameter	Typical Value		Impedance at f = 4 GHz
g_c	10	umho	100k Ω
C_c	0.25	Pf	160 Ω
C_b	0.40	Pf (V = 0)	100 Ω (V = 0)
R_b	3.0	Ω (Low Frequency)	--
r_s	0.80	Ω ($f \cong$ 8 GHz)	0.80 Ω
L	0.8	nanohenry	20 Ω

Since we are interested in power levels on the order of tenths of a watt at impedance levels of 50 to 377 ohms, diode behavior in the forward current range of tens to hundreds of milliamperes is important. A typical current-voltage curve for a hot carrier diode in this range is shown in Figure 14.



Here, V_F would be taken as 0.60 volt and R_F as 1.4 ohms

Figure 14. Oscilloscope Trace of a Typical Hot Carrier Diode Forward Characteristic in the Current Range of 0 - 100 mA

It is readily seen that the characteristic no longer follows the diode equation at these high currents and it becomes more meaningful, from a circuit standpoint, to consider the linearized approximation given in Figure 15. Here, we characterize the forward characteristic by the two parameters V_F and R_F. The former is simply the voltage axis intercept of the actual characteristic extrapolated backward from the 100 and 50 mA points, while the latter is just $R_b + r_s$, as can be seen from the equivalent circuit.

2.3 DIODE LOSSES

On the basis of the equivalent circuit of Figure 12 and the approximate values given in Table I we now make the following assumptions:

(a) During the forward conduction part of the cycle the junction capacitance is effectively short circuited.

(b) The reactances of the diode(s) are compensated for by the input filter in such a way that the idealized waveforms derived in the previous section are still good approximations to the actual waveforms.

(c) The losses are not so great that the idealized waveforms are significantly distorted; i.e., currents and voltages which are associated with losses are small compared with the idealized currents and voltages.

(d) g_c may be ignored.

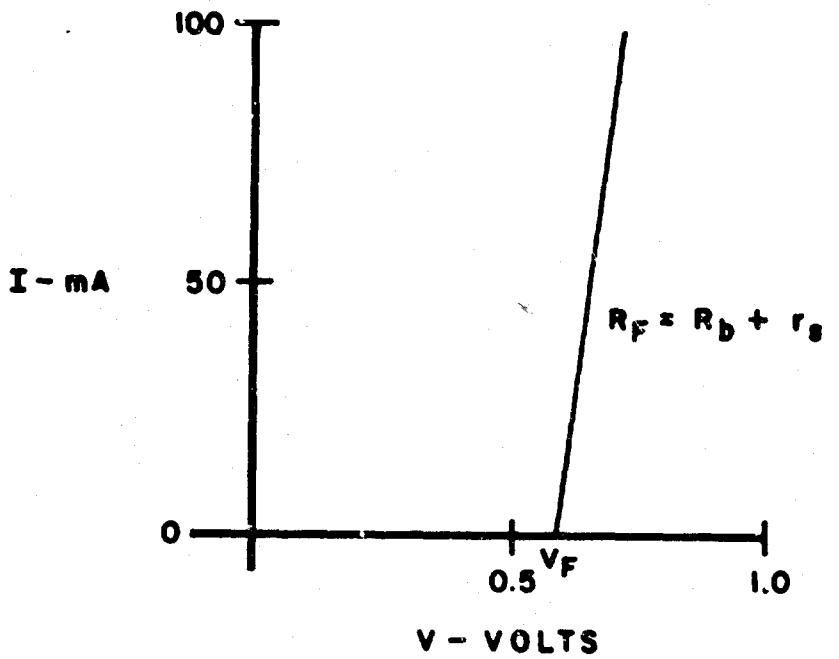


Figure 15. Linearized Current - Voltage Curve

Thus, we may consider three distinct loss mechanisms in the diode (aside from minority carrier effects, which are discussed in a later section):

(1) Loss due to the forward voltage drop, V_F.
(2) Loss due to the forward resistance, R_F.
(3) Loss due to reverse conduction through C_b, r_s, and L.

These will be considered in turn for the circuits previously analyzed. However, in view of the fact that all of our actual circuits have output filtering more closely resembling the shunt capacitor case, only such circuits will be analyzed here.

2.3.1 Full-Wave Bridge With Series Input and Shunt Capacitor Output Filters

Under the assumptions just listed we see that the fundamental current passing through each diode causes a loss given by

$$\frac{1}{\pi}\int_{\pi}^{\pi} V_F i(\omega t)d(\omega t) = \frac{E_P V_F}{2\pi R_G}\int_{0}^{\pi} \sin x\, dx = \frac{E_P V_F}{\pi R_G} \tag{99}$$

due to the forward drop, V_F. Since this current passes through two diodes in series, the total loss due to this cause is,

$$P_1 = \frac{2E_P V_F}{\pi R_G} = \frac{E_P^2}{8R_G}\left(\frac{16V_F}{\pi E_P}\right) = \frac{E_P^2}{8R_G}\left(\frac{2V_F}{E_{DC}}\right) \tag{100}$$

Similarly, there is a loss in each diode due to R_F given by

$$\frac{1}{\pi}\int_{0}^{\pi} R_F\, i^2(\omega t)d(\omega t) = \frac{E_P^2 R_F}{4\pi R_G^2}\int_{0}^{\pi} \sin^2 x\, dx = \frac{E_P^2 R_F}{8R_G^2} \tag{101}$$

so that the total loss due to R_F in the two conducting diodes is

$$P_2 = \frac{E_P^2 R_F}{4R_G^2} = \frac{E_P^2}{8R_G} \left(\frac{2R_F}{R_G}\right) \tag{102}$$

The reverse conduction losses are somewhat more difficult to estimate. Each diode is subjected to a square wave voltage pulse of amplitude E_{DC} and duration $T = \frac{1}{2f}$ in the reverse direction, where f is the operating frequency. During the time that this reverse voltage pulse is applied the diode equivalent circuit reduces to that shown in Figure 16.

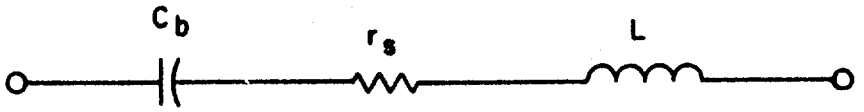


Figure 16. Diode Equivalent Circuit During Reverse Conduction

The current through this circuit under the application of a step voltage input given by

$$v(t) = \begin{cases} 0 & , t<0 \\ E_{DC}, & t\geq 0 \end{cases} \tag{103}$$

is

$$i(t) = \frac{E_{DC}}{\omega_o L} e^{-t/\tau} \sin \omega_o t \tag{104}$$

where:

$$\tau = 2\frac{L}{r_s} \; ; \; \omega o = \frac{1}{\sqrt{L\, C_b}}.$$

If we substitute the values given by Table I in the above we find that

$$\tau \cong 2 \text{ ns}$$

$$f_o = \frac{\omega_o}{2\pi} \cong 9 \text{ GHz} \tag{105}$$

Since τ is considerably greater than $T = \frac{1}{2f}$, the OFF period for the diode, we may ignore the exponential decay in equation 104 and write,

$$i(t) \cong \frac{E_{DC}}{\omega_o L} \sin \omega_o t, \quad 0 \leq t \leq T. \tag{106}$$

Now, when the pulse shuts off, that is when the diode starts to conduct in the forward direction, the above current will exponentially decay with a time constant given approximately by $L/R_F \sim 0.2$ ns, but at this time the two remaining diodes become back biased and a current given by equation 106 flows in them. Thus, such a current is always flowing in two diodes and if we ignore the loss in the decay and the complicated phase relationships involved we may estimate the total loss due to reverse conduction as

$$P \cong \frac{2}{\pi} \int_0^{\pi} r_s \, i^2 \, (\omega_o t) \, d \, (\omega_o t) = 2 \frac{E_{DC}^2 \, r_s C_b}{\pi L} \int_0^{\pi} \sin^2 x \, dx$$

$$= \frac{E_{DC}^2 r_s C_b}{L} = \frac{E_P^2}{8R_G} \left(\frac{\pi^2 R_G r_s C_b}{8L}\right) \tag{107}$$

where: $E_{DC} = \frac{\pi}{8} E_P$ have been used.

$$\omega_o = \frac{1}{\sqrt{LC_b}}$$

At this point we may estimate the percentage losses due to each of the above mechanisms, where we let

$$R_G = 377\ \Omega$$
$$V_F = 0.5 \text{ volt}$$
$$E_{DC} = 10 \text{ volts.}$$

Thus,

$$\frac{P_1}{P_A} = 2\,\frac{V_F}{E_{DC}} \cong 10\%$$

$$\frac{P_2}{P_A} = 2\,\frac{R_F}{R_G} \cong 2\%$$

$$\frac{P_3}{P_A} = \frac{\pi^2 R_G r_s C_b}{8L} \cong 18.6\%$$

giving a total theoretical efficiency of

$$\eta \cong 69.4\%$$

2.3.2 Full-Wave Bridge With Shunt Input and Shunt Capacitor Output Filters

Since the current waveform ideally approaches that of a delta function any estimate of the forward conduction losses must depend upon some knowledge of the actual, nonideal waveform. The task of calculating this waveform in the presence of the parasitic elements presented by the diodes is probibitively complicated so we will content ourselves with the following approximate analysis.

As an approximation to the actual current waveform we adopt a rectangular pulse of width ϵ and height Q/ϵ, where Q is the total charge transferred per half cycle. While an infinitely fast rise time would in practice be prohibited by the diode series inductance, L, one can expect that the error involved in the loss calculations based upon this waveform will be small for reasonably narrow pulses, that is, the actual form of the pulse is not critical, only its height to width ratio, Q/ϵ^2.

Thus, we find for the loss due to V_F in each conducting diode,

$$\frac{1}{\pi}\int_0^{\pi} V_F i(\omega t)\,d(\omega t) = \frac{V_F\ Q\omega}{\pi} \tag{108}$$

Putting in the expression for $Q = \dfrac{\pi\ E_{DC}}{\omega\ R_L}$ (109)

and multiplying by two, we obtain the total loss in both diodes due to V_F,

$$P_1 = \frac{E_{DC}^2}{R_L}\left(\frac{2V_F}{E_{DC}}\right) = \frac{E_P^2}{8R_G}\left(\frac{2\ V_F}{E_{DC}}\right) \tag{110}$$

which is identical with equation (100).

For the loss due to R_F in each diode we have,

$$\frac{1}{\pi}\int_0^{\pi} R_F i^2(\omega t)\,d(\omega t) = \frac{R_F \omega Q^2}{\pi\epsilon} \tag{111}$$

and making the same substitution as above for Q we find for the total loss due to R_F,

$$P_2 = \frac{2\pi R_F \, E_{DC}^2}{\epsilon \omega R_L^2} \tag{112}$$

Expressing the product $\epsilon\omega$ in terms of the conduction angle, ϕ, defined earlier,

$$\epsilon\omega = 2\,\phi \tag{113}$$

we have,

$$P_2 = \frac{E_{DC}^2}{R_L}\left(\frac{\pi R_F}{\phi R_L}\right) = \frac{E_P^2}{8R_G}\left(\frac{\pi R_F}{2\phi R_G}\right) \tag{114}$$

where we have used the relation, $R_L = 2R_G$.

Here, we see that the loss varies inversely with the conduction angle, ϕ, so that the narrower the current pulse, the greater the loss.

To calculate the reverse conduction losses we assume that the conduction angle is sufficiently small that all four diodes in the bridge may be considered to be in the OFF state throughout most of the cycle. Then, each diode equivalent circuit reduces to that shown in Figure 16, and since the four diodes appear in series parallel combination across the line, the resultant impedance is simply that of a single diode in the OFF state.

The admittance of this circuit is given by

$$Y = \frac{r_s}{r_s^2+(\omega L-\frac{1}{\omega C_b})^2} - j\,\frac{\omega L-\frac{1}{\omega C_b}}{r_s^2+(\omega L-\frac{1}{\omega C_b})^2} = G - jB \tag{115}$$

and as before, we assume that the input filter is tuned so that the reactive part of the total admittance (including the case capacitance, not included in the above) vanishes. Then, the loss is given by

$$P_3 = \left(\frac{E_1}{2}\right)^2 G = \frac{E_P^2}{8R_G} \quad (2R_G \alpha g_s^2 r_s) \tag{116}$$

where:

$$G = \alpha g_s;\ g_s = \frac{1}{r_s}\ ;\ \alpha = \frac{1}{1+\left(\frac{\omega L - \frac{1}{\omega C_b}}{r_s}\right)^2}.$$

We see that operation near resonance, $\omega L = \frac{1}{\omega C_b}$, must be avoided if this loss term is to remain small, and under these conditions we may write

$$\alpha \cong \frac{r_s^2}{\left(\omega L - \frac{1}{\omega C_b}\right)^2} \tag{117}$$

In Figure 17 we have plotted the function αg_s^2 for various values of L and C_b. The branch of the function above resonance has been omitted for clarity. The advantage of a small capacitance is clear from these curves.

We may estimate the loss due to the above by using the typical diode parameters listed in Table I and choosing R_G = 377 ohms, f = 4 GHz. Then we find $\alpha g_s^2 \cong 2 \times 10^{-4}$ mho^2 and,

$$\frac{P_3}{P_A} \cong 12\%$$

For the R_F losses we have no way of estimating the conduction angle, ϕ, but just as an example we assume a value of $\phi = \frac{\pi}{20}$ = 9 degrees.

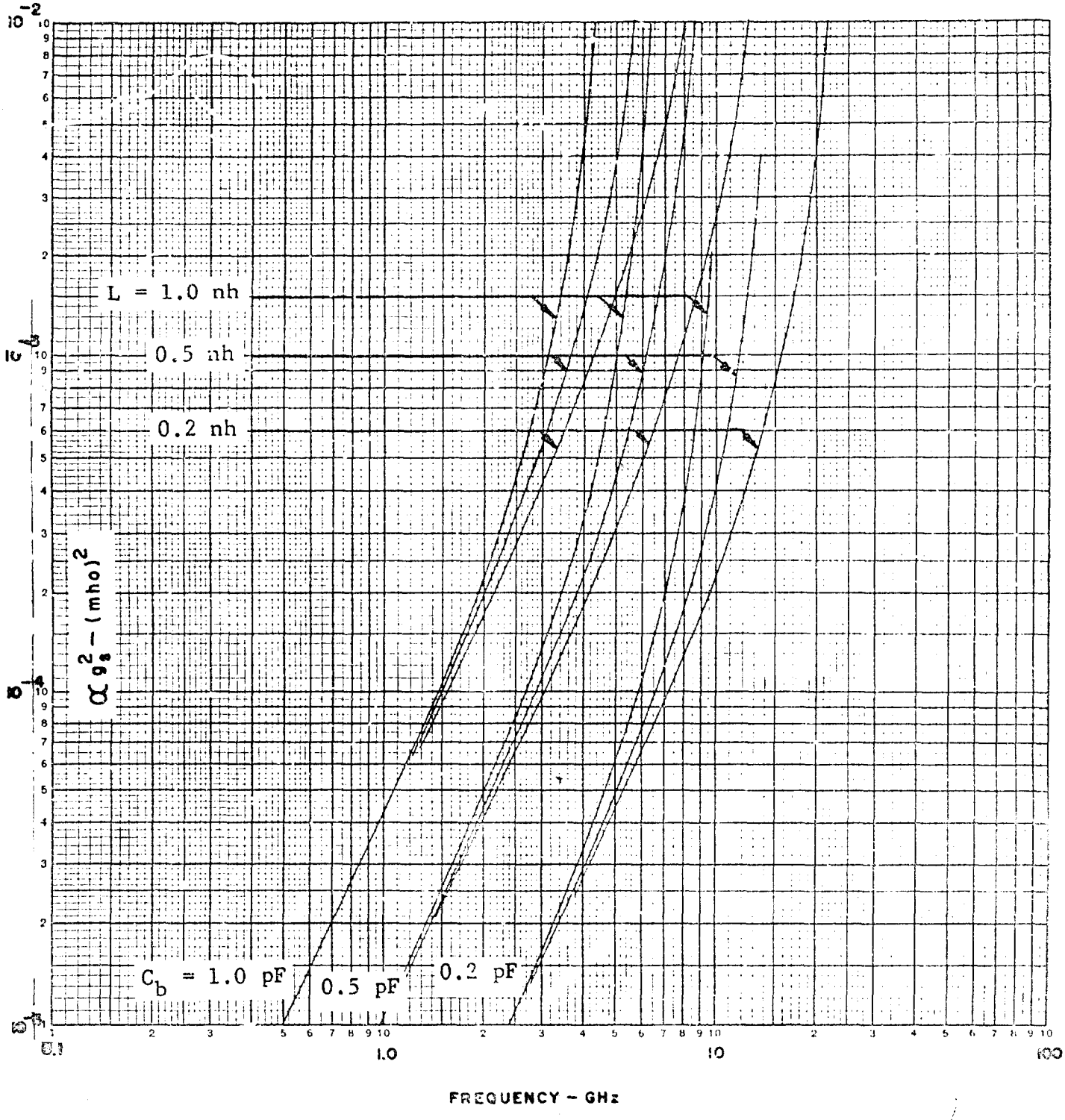


Figure 17. The Loss Function, $\alpha\, g_s^2$, as a Function of Frequency for Various Reactive Diode Parasitics

Then,

$$\frac{P_2}{P_A} \cong 10\%$$

and taking into account the 10% V_F loss previously obtained we find a theoretical efficiency of,

$$\eta \cong 68\%.$$

2.3.3 Half-Wave Circuit With Shunt Input Filter

As noted in the previous analysis for this circuit, the total charge contained in the current pulse is twice that for the full-wave circuits, but since there is only a single diode through which this flows, the total loss due to V_F is the same as before,

$$P_1 = \frac{E_P^2}{8R_G} \left(\frac{2V_F}{E_{DC}}\right). \tag{118}$$

However, since the R_F loss varies as the square of the charge, Q, this component will be double that found for the corresponding full-wave case, so that

$$P_2 = \frac{E_P^2}{8R_G} \left(\frac{\pi R_F}{\phi R_G}\right) \tag{119}$$

Finally, the reverse conduction losses can be seen to be the same as the corresponding full-wave case since the single diode presents the same equivalent impedance as before, and the voltage amplitude is the same in each case. Hence,

$$P_3 = \frac{E_P^2}{8R_G} \left(2R_G \alpha g_s^2 r_s\right) \tag{120}$$

We will not treat the series input filter, half-wave case here since the input voltage waveform for this circuit involves a high voltage spike which the actual diode cannot tolerate.

2.4 Q LOSSES

The equivalent circuit for a shunt filter with loss is shown in Figure 18.

The impedence for this circuit is given by,

$$Z = \frac{1}{Y} = \frac{1}{j\omega C' + \frac{1}{r+j\omega L}} = \frac{1}{j\omega C' + \frac{r-j\omega L}{r^2+\omega^2 L^2}} = \frac{r^2 + \omega^2 L^2}{j\omega C'(r^2\omega^2 L^2)+r-j\omega L}$$

$$= \frac{r^2 + \omega^2 L^2}{r+j\omega C'(r^2+\omega^2 L^2-\frac{L}{C'})} \qquad (121)$$

At $\omega = \omega_o$, where

$$X = \omega_o L = \frac{1}{\omega C'}; \quad Q = \frac{\omega_o L}{r} = \frac{X}{r}, \qquad (122)$$

$$Z(\omega_o) = \frac{r^2+\omega_o^2 L^2}{r+j\frac{r^2}{\omega_o L}} = r\,\frac{1+Q^2}{1+j\frac{1}{Q}}, \qquad (123)$$

and for $Q >> 1$,

$$Z(\omega_o) \cong rQ^2 = XQ \qquad (124)$$

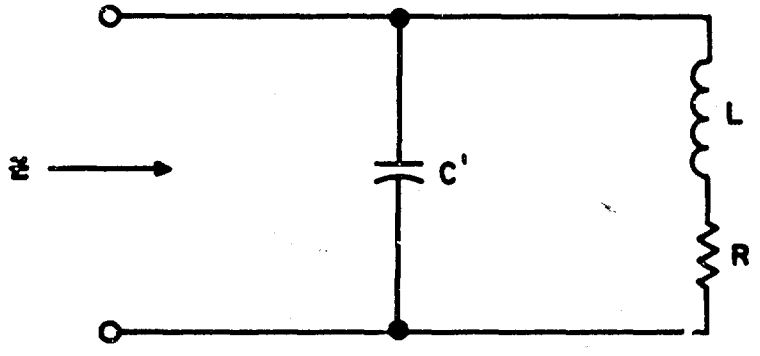


Figure 18. Equivalent Circuit for Shunt Filter with Loss

At the third harmonic,

$$Z(3\omega_o) = \frac{r^2 + 9\omega_o^2 L^2}{r + j3\omega_o C'(r^2 + 8\omega_o^2 L^2)} = r\,\frac{1 + 9Q^2}{1 + j\frac{3}{Q}(1 + 8Q^2)}\,, \qquad (125)$$

and for $Q \gg 1$ this is purely capacitive and,

$$\boxed{\left|Z(3\omega_o)\right| \simeq \frac{9}{24}\,rQ = \frac{9}{24}\,X} \qquad (126)$$

Under the assumption of small losses in the circuit, the loss at the fundamental is given by,

$$P_\ell = \frac{E_P^2}{8Z(\omega_o)} \qquad (127)$$

Hence, the percentage loss is,

$$\frac{P_\ell}{P_A} = \frac{E_P/8Z(\omega_o)}{E_P^2/8R_G} = \frac{R_G}{Z(\omega_o)} \simeq \frac{R_G}{QX} \qquad (128)$$

Note that if the filter is to provide a good short circuit to the third harmonic, X must be small compared with the characteristic impedance R_G. As an example, if,

$$\frac{\left|Z(3\omega_o)\right|}{R_G} = \frac{\frac{9}{24}\,X}{R_G} = \frac{9X}{24R_G} = 0.01, \text{ then,} \qquad (129)$$

$\frac{P_\ell}{P_A} = \frac{1}{Q}\,\frac{100}{24} \simeq \frac{4}{Q}$, and one requires a Q greater than 400 for this to be less than 1 percent, which should be readily achievable at microwave frequencies.

However, at ω_o = 4 GHz a shunt capacitance of 1 pF corresponds to an X of ~ 37 ohms so that $X/R_G = 0.1$ for a 377-ohm line and for a Q = 400,

$$\frac{P_\ell}{P_A} \cong 2.5 \text{ percent.}$$

2.5 DISCUSSION OF LOSSES

An approximate analysis of the losses present in various "practical" rectifier circuits has been given, based upon the diode equivalent circuit shown in Figure 12. At best, this can serve only as a guide since the actual circuits operating in the microwave range will not necessarily correspond to any of those treated.

Thus, for example, the actual filtering arrangement may be more complicated than the simple L-C combinations chosen for the analysis and their filtering properties may lie intermediate to the idealizations used.

Nevertheless, the following observations may be made:

(1) The percentage loss brought about by the forward voltage drop of the diode expressed in terms of the output voltage, E_{DC}, is the same in all circuits. In fact, it is easy to show that this loss component is independent of the form of the input current waveform.

(2) The percentage loss due to the diode forward resistance becomes greater as the input current waveform becomes sharper, i.e., more pulse-like.

(3) In general, the losses will be lower if R_F, r_s, and C_b are kept as small as possible. The effect of the diode inductance, L, appears to depend critically upon the input filtering circuit.

SECTION III

3.0 DIODE DESIGN

3.1 INTRODUCTION

In this section we discuss the essential features of the hot carrier diode design as they relate to the considerations of efficiency dealt with in preceding sections. Since the general theory has been adequately discussed in the literature, as far as it has been developed, this aspect will not be treated here.

3.2 PHYSICAL STRUCTURE

The physical structure of the diode is shown in Figure 13 of Section 2.2. The silicon chip is 0.007 inch thick, 0.0005 to 0.0009 ohm-cm N-type material on which an epitaxial layer several tenths of a micron is deposited. A 1-micron SiO_2 glass is deposited on top of this and the active area etched by standard photoresist techniques. After suitable cleaning a metallized layer is deposited on the exposed silicon surface, thus forming a metal-semiconductor junction. This is then etched to form bonding areas, final contact being made either directly to the pad, or to a gold-plated contact formed on the pad area.

Details of the metallization will be discussed in the next section.

3.3 IMPURITY CONCENTRATION PROFILE

To minimize the series resistance of the diode it is necessary to design it so that the spreading resistance is due to low resistivity material only. The most ideal way of doing this would be to adjust the epitaxial layer doping level and thickness

so that at zero bias the junction depletion layer would extend into the very heavily doped substrate material.

Unfortunately, this cannot be done since the doping in the thin epitaxial layer is determined largely by outdiffusion from the substrate, in spite of the fact that the layer is grown at the lowest possible temperature. Thus, one cannot maintain a constant impurity concentration in the epitaxial layer and a graded junction results.

In view of this, the next best procedure is to make this gradient as steep as possible so as to minimize the contribution to the spreading resistance by the epitaxial layer, and this is the procedure we have followed.

An example of a typical impurity distribution is provided by the profile shown in Figure 19. This data was obtained by beveling a sample wafer and making resistivity measurements along the bevel by means of a two-point probe. Since the bevel angle is known, position along the bevel can be directly related to depth from the surface.

However, this method is limited since an unknown amount of probe penetration takes place. For this reason, the concentration near the surface is in doubt, and to shed some additional light on this a series of capacitance-voltage measurements was made under conditions of forward bias. By means of the Schottky capacitance relation and the simple capacitance-depth formula these were then translated into a profile. The results were somewhat surprising as shown in Figure 20, where the two point probe data is combined with that obtained from the capacitance-voltage measurements to give an overall profile. The C-V data provides information down to a depth of about 650 Å and the two-point probe from there down.

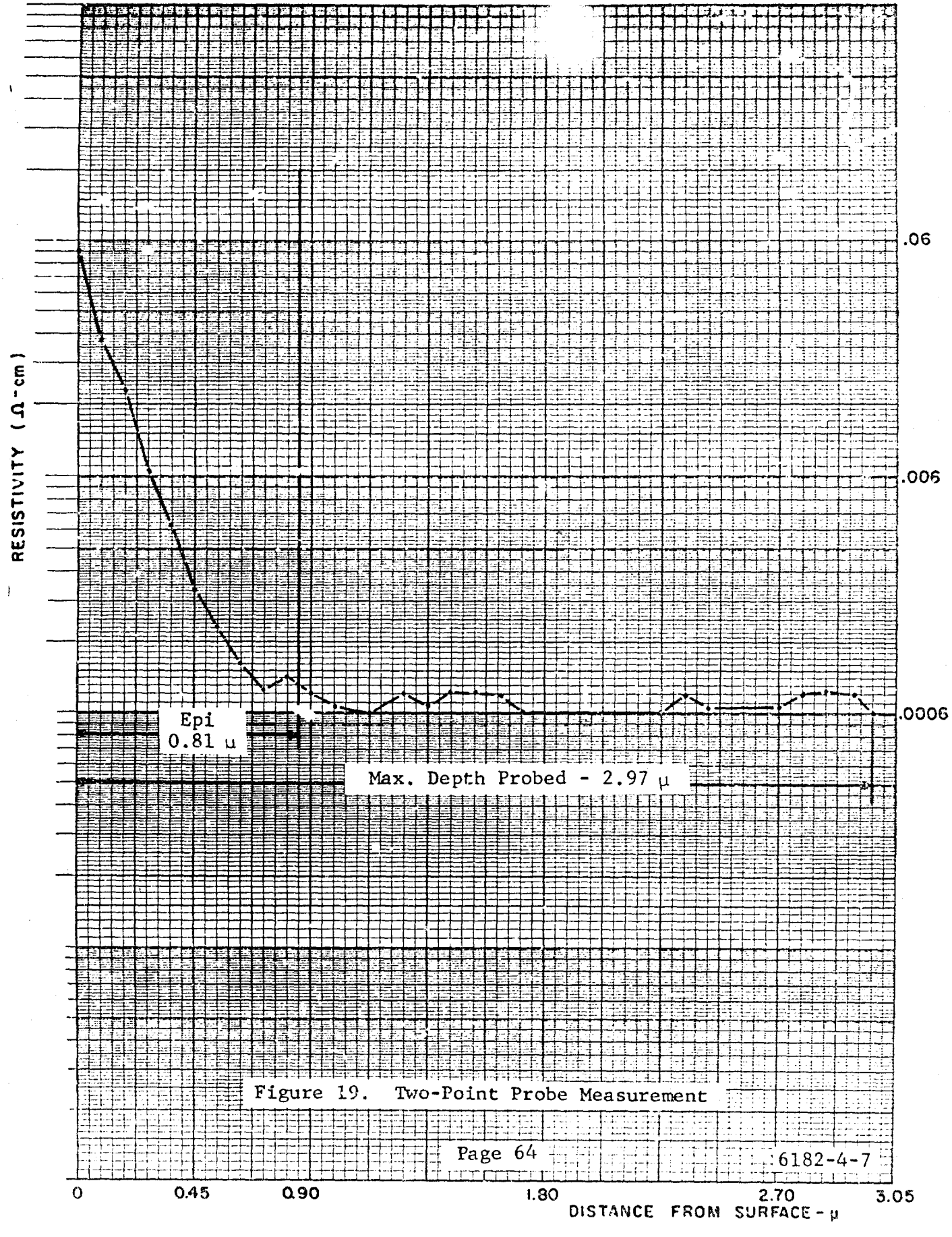


Figure 19. Two-Point Probe Measurement

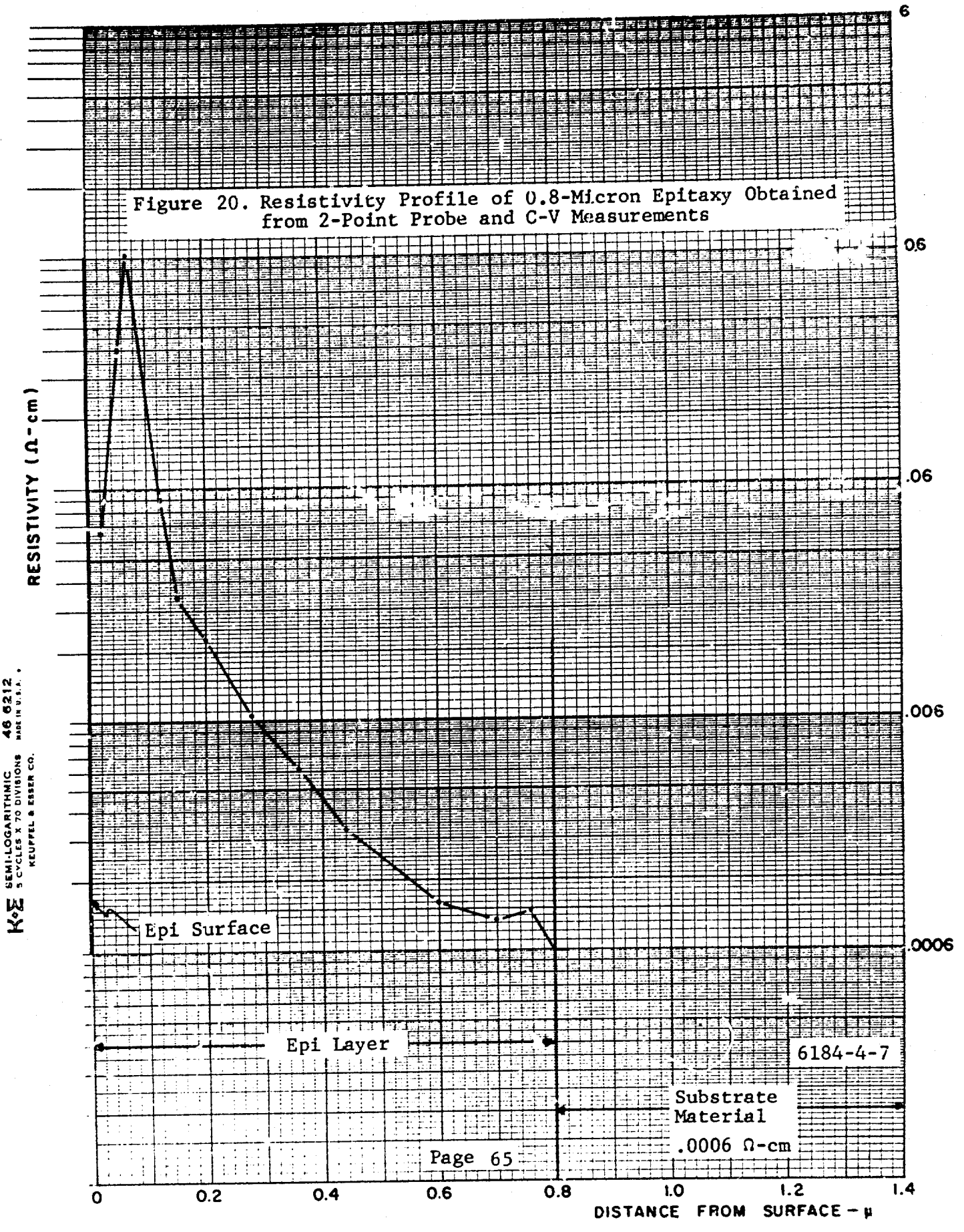


Figure 20. Resistivity Profile of 0.8-Micron Epitaxy Obtained from 2-Point Probe and C-V Measurements
RESISTIVITY (Ω-cm)
6
.6
.06
.006
.0006
Epi Surface
Epi Layer
6184-4-7
Substrate Material
.0006 Ω-cm
0
0.2
0.4
0.6
0.8
1.0
1.2
1.4
DISTANCE FROM SURFACE – μ
K&E SEMI-LOGARITHMIC 5 CYCLES X 70 DIVISIONS KEUFFEL & ESSER CO. 46 6212 MADE IN U.S.A.

It can be seen that instead of the expected steady increase in resistivity as one proceeds toward the surface, one finds a maximum resistivity at a depth of ~650 Å and a decrease from there to the surface. No satisfactory explanation for this phenomenon was found, but measurements made on some competitive devices show a similar variation.

It is possible that the C-V data is being misinterpreted in these measurements. First of all, it is necessary to make the capacitance measurements with the diode in a fairly high conductance state to obtain information close to the surface barrier. A further complication arises from an anomalous frequency-capacitance relationship which forces one to rely on low frequency measurements. This is shown in Figure 21, where the capacitance is plotted as a function of frequency for several different forward voltages. (The measurements were made with the circuit shown in Figure 22, using a Boonton type 250-A R-X Meter.) Here it can be seen that at high frequencies and high forward bias the capacitance has a substantial frequency dependence. Similar results have apparently been obtained in the past[1] with point contact diodes and the phenomenon is believed to be due to relaxation effects within the depletion layer. Indeed, it may be that such effects play a very important role in the rectification process at microwave frequencies.

These C-V measurements were made at a frequency of 10 MHz. At this frequency one is faced with the problem of measuring the minor component of a low Q circuit since the capacitive susceptance is much smaller than the diode conductance at the forward bias voltages necessary for shallow probing.

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(1) H. K. Henisch, Rectifying Semiconductor Contacts, Oxford University Press, 1957, pp. 166-7, 270-2.

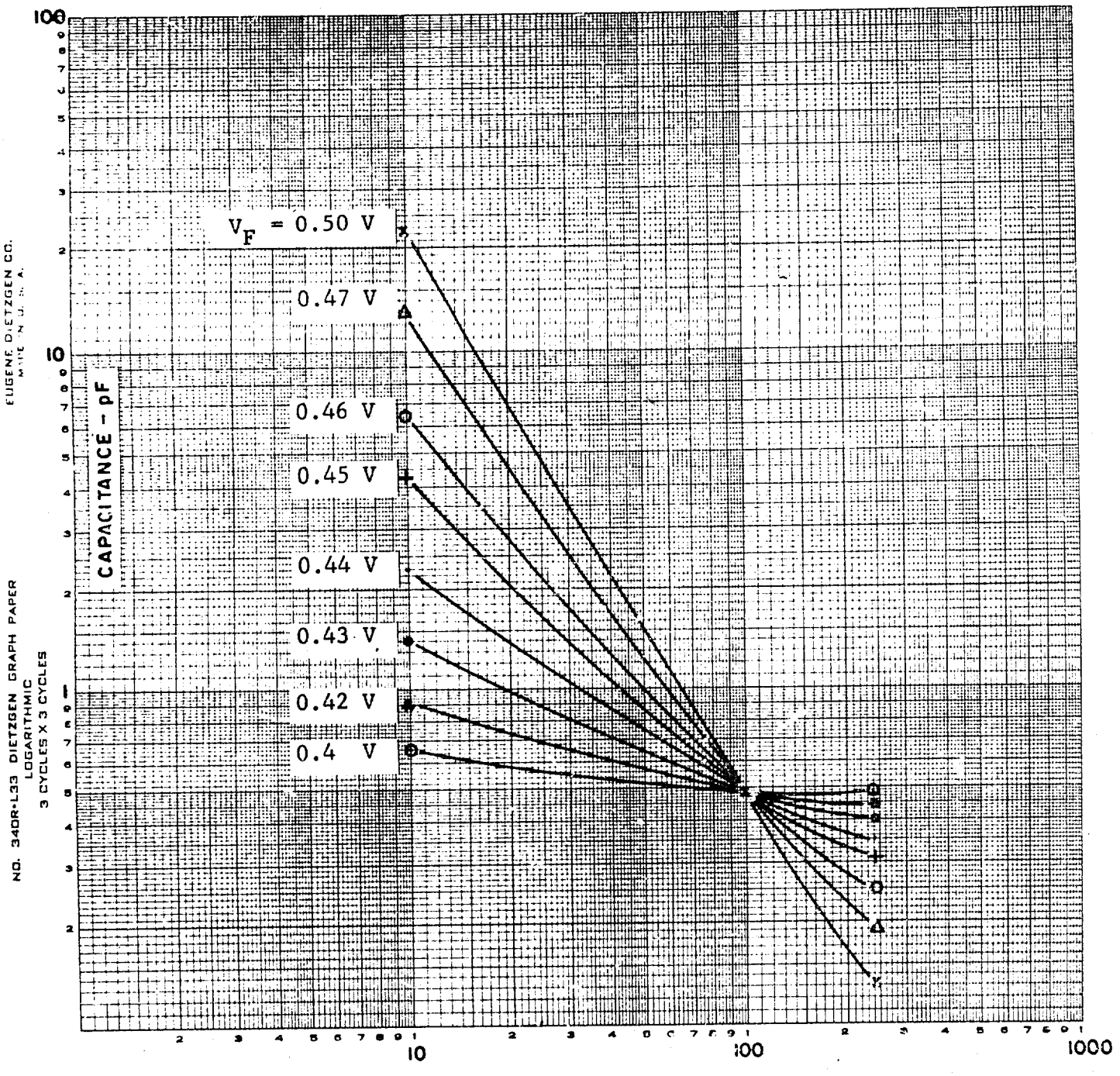

Figure 21. Experimental Data of C_b vs f with Forward Bias as a Parameter

6280-5-7

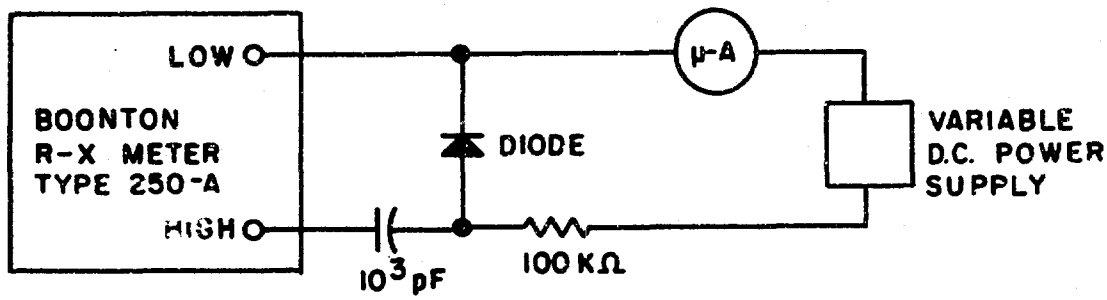

Figure 22. Circuit Used for Measuring C_b

In view of these uncertainties in the measurements the impurity concentration near the surface of the diode must remain in question.

SECTION IV

4.0 DIODE METALLIZATION

4.1 INTRODUCTION

The experimental hot carrier diodes fabricated in our laboratories prior to the initiation of this contract utilized an ultrahigh vacuum evaporation process for the deposition of the contact metal. The rather long cycle time associated with this procedure made it desirable to seek a more efficient means of accomplishing this and consequently a short investigation of alternate schemes was carried out at the start of this program.

A molybdenum-gold metallization had been found highly satisfactory in the past, so our main effort was concerned with alternate methods of depositing this combination, although some work was also carried out using the metals chromium, aluminum, and tungsten. The Mo-Au contact is always deposited so that only pure Mo forms the Schottky barrier, the Au being deposited on top of the Mo and serving the dual function of protecting the Mo from oxidation and allowing standard wire bonding techniques to be employed. To insure a low resistance contact, the two metals, which are deposited from independent sources in the evaporator, are blended at the interface by starting the Au evaporation just prior to the conclusion of the Mo evaporation. This technique prevents the formation of any oxide at the Mo-Au interface. This is an important consideration since the deposition must be carried out on a substrate held at an elevated temperature (typically 300°C) to secure good adhesion of the Mo, and in all but ultrahigh vacuum systems, oxidation could proceed under these circumstances.

4.2 TRIODE SPUTTERING VS ELECTRON BEAM EVAPORATION

In our investigation, we looked into the use of low pressure triode sputtering with argon[2] and electron beam evaporation in an oil diffusion pumped vacuum system operating in the 10^{-6} torr range. Each of these methods has produced quite satisfactory results with Mo-Au and Cr-Au, although as discussed below, the latter has certain disadvantages from our point of view. Thus, it seems that a choice between the two methods of deposition may be made on the basis of convenience, both methods being far more convenient and quicker than the one using an ultrahigh vacuum evaporator.

In the case of sputtering, one has the option of applying a dc bias voltage to the substrate prior to and during the deposition process. This should allow a cleanup of the silicon surface immediately before the Mo contacts it and should provide a gas desorption cleaning during the deposition of the Mo so that a purer metal is formed.

That such a cleaning does in fact take place is made clear by the electron micrograph shown in Figure 23. Here an excessive bias has been applied to the substrate and actual removal of the Si has resulted. This etching of the Si has an adverse effect upon the breakdown voltage of the diodes since there exists a rather steep impurity concentration gradient in the epitaxial layer of the device which results in the formation of a contact on lower resistivity material. Thus, one must carefully control the substrate bias to secure the desired surface cleaning without actually removing the Si itself.

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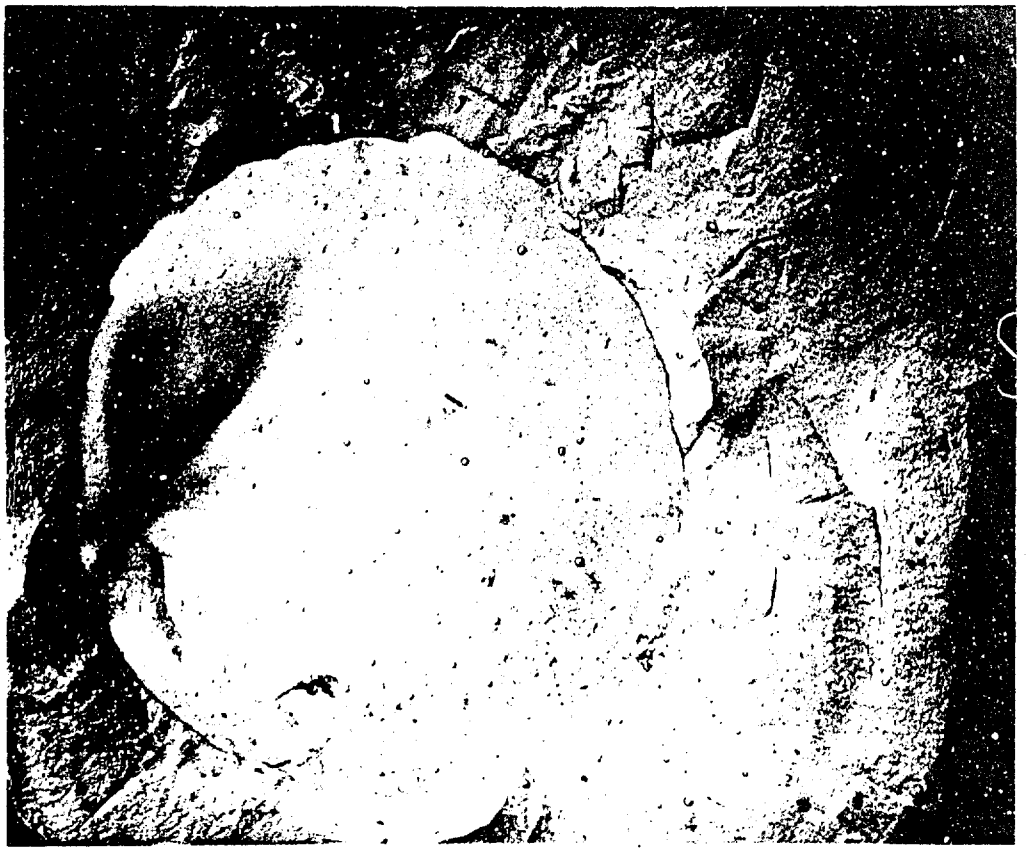
[2] Symposium on Deposition of Thin Films by Sputtering, University of Rochester and Consolidated Vacuum Corporation, June 6, 1966.



5000 X

NOTE: Surrounding area is deposited SiO_2 glass.

Figure 23. Electron Micrograph of Replica of Sputtered Diode Area Showing Damage Due to Excessive Substrate Bias

It was originally felt that this cleanup ability of the sputtering technique would make it superior to ordinary electron beam evaporation at 10^{-6} torr, but experience has not shown this to be the case as the two methods produce essentially the same results. This can be seen by comparing Figures 24 and 25, which show typical current-voltage curves for diodes prepared by the two methods. In the particular case shown in Figure 25, the reverse voltage is rather low, but this problem periodically appears independently of the deposition method used and may be associated with the epitaxial layer itself rather than the contact formation.

4.3 DIFFERENT METALS

As mentioned above, the results with chromium as a contact metal were roughly equivalent to those obtained using molybdenum. However, in one important respect they are not equivalent; this is in the forward voltage drop in the 10 to 100 mA current range. This is important because the ability to achieve high ac to dc conversion efficiency requires operation at these high currents and beyond.

For some reason not presently understood, Cr consistently produces diodes having higher forward voltage at 100 mA than does Mo. The current voltage characteristic for a typical Cr contact diode is shown in Figure 26, which shows that at currents below about 1.0 mA Cr is equivalent to Mo. Nevertheless Cr has a considerably higher forward voltage drop at higher currents.

Since aluminum is one of the metals most commonly used in the semiconductor industry for contacts and conductors, this metal was also tried as a contact for hot carrier diodes. A typical result is shown in Figure 27. Essentially the same comment just made regarding Cr can also be made with respect to Al. Al exhibits a superior performance to Mo at currents below 1.0 mA and a far poorer one at higher values.

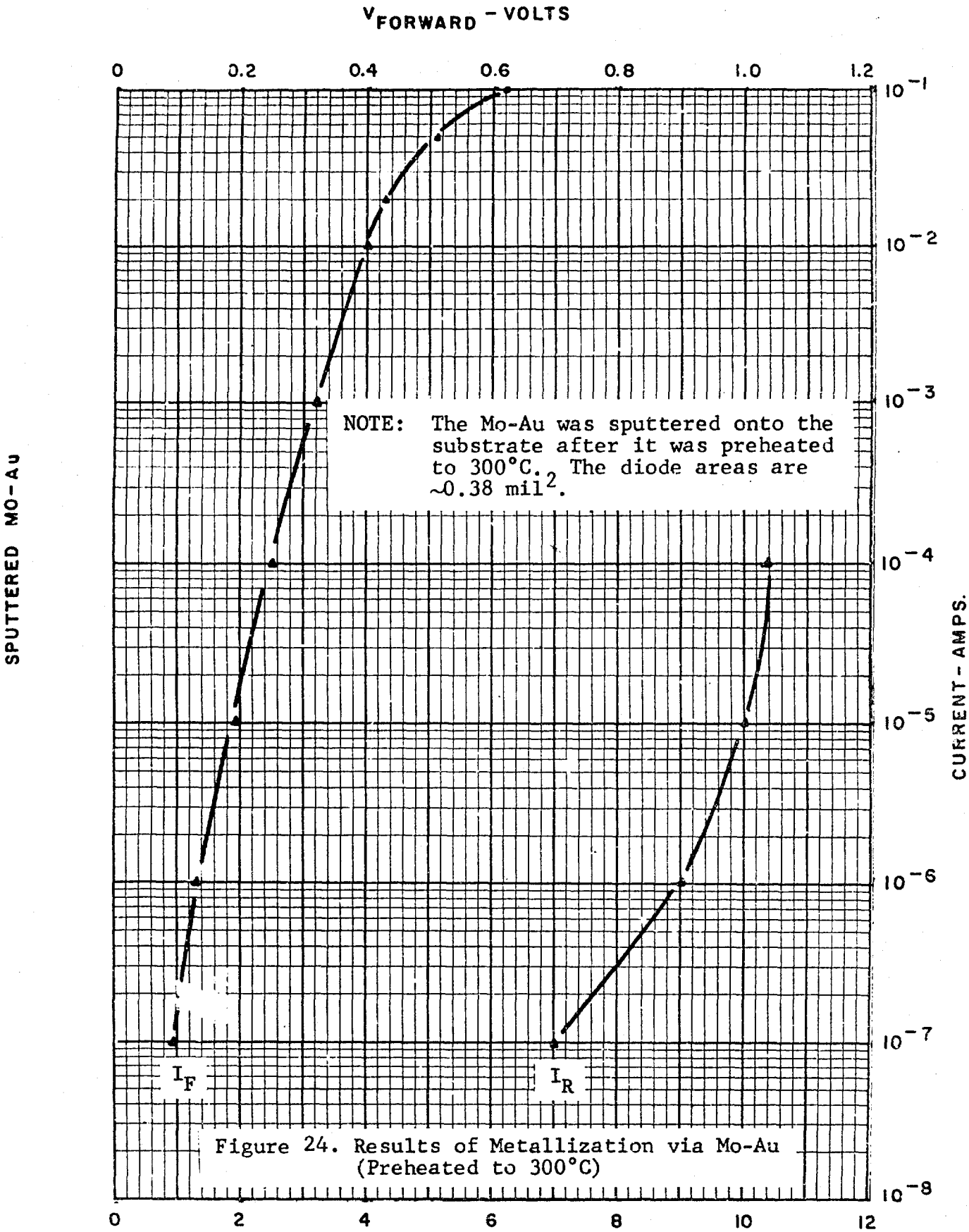


Figure 24. Results of Metallization via Mo-Au (Preheated to 300°C)

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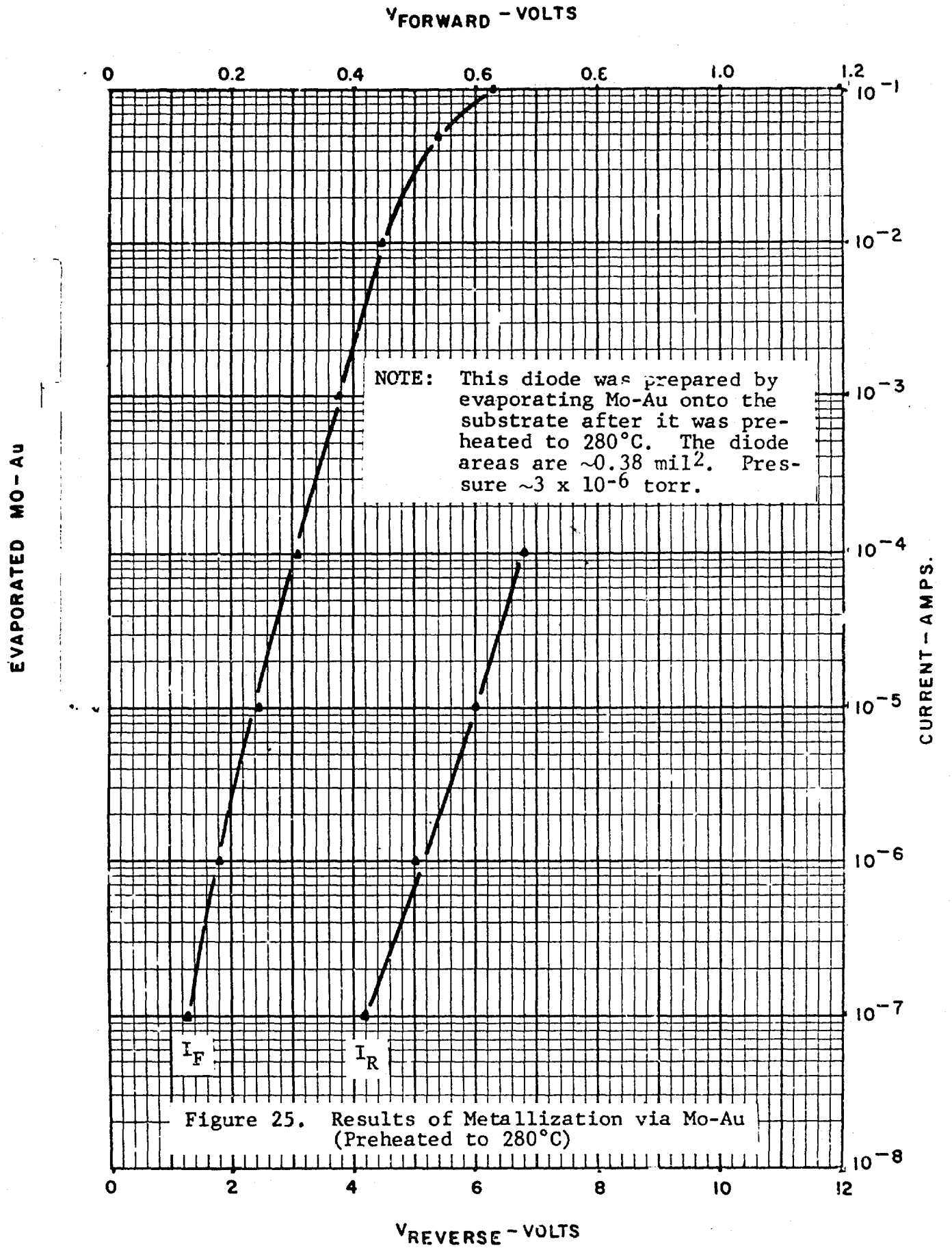

Figure 25. Results of Metallization via Mo-Au (Preheated to 280°C)

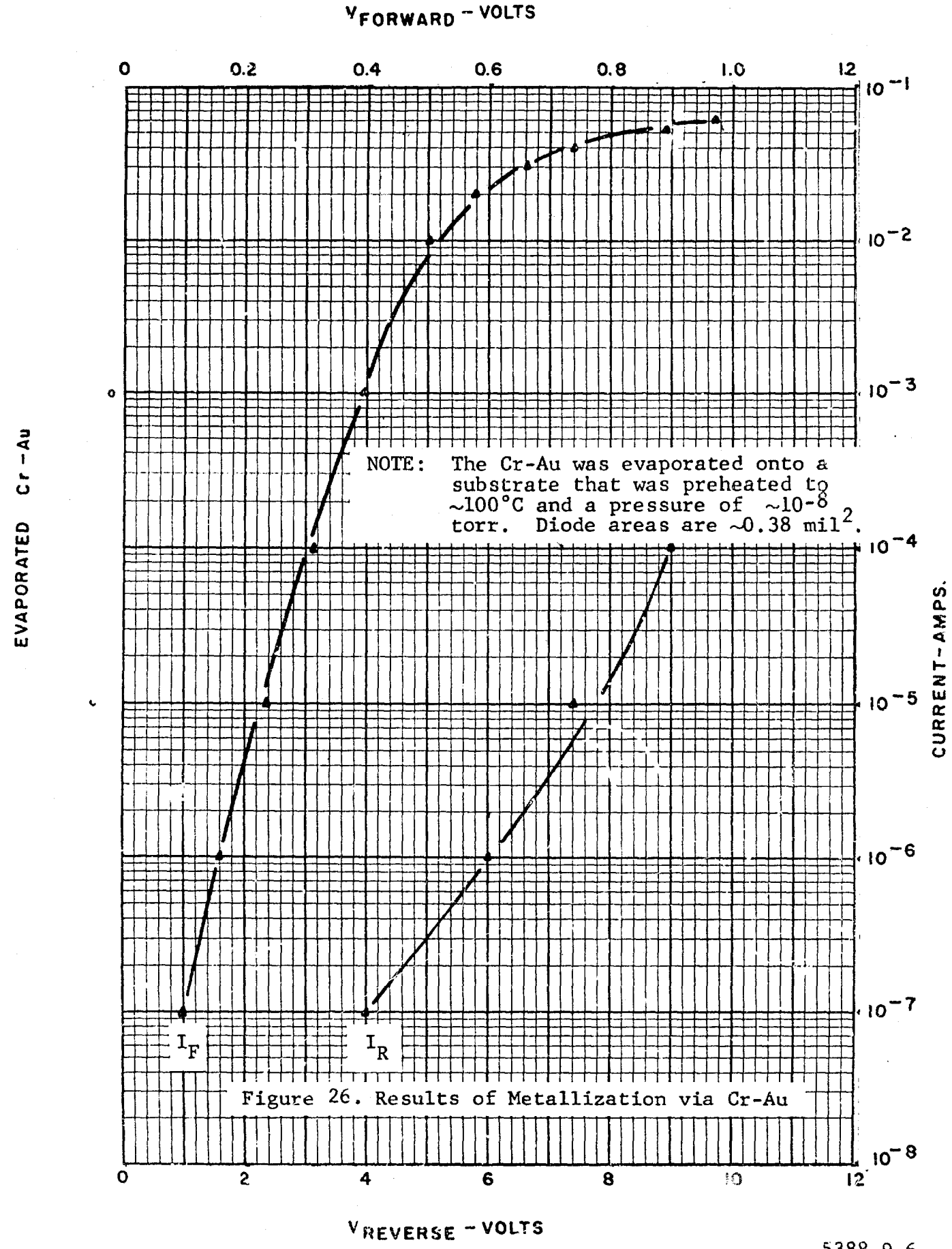

Figure 26. Results of Metallization via Cr-Au

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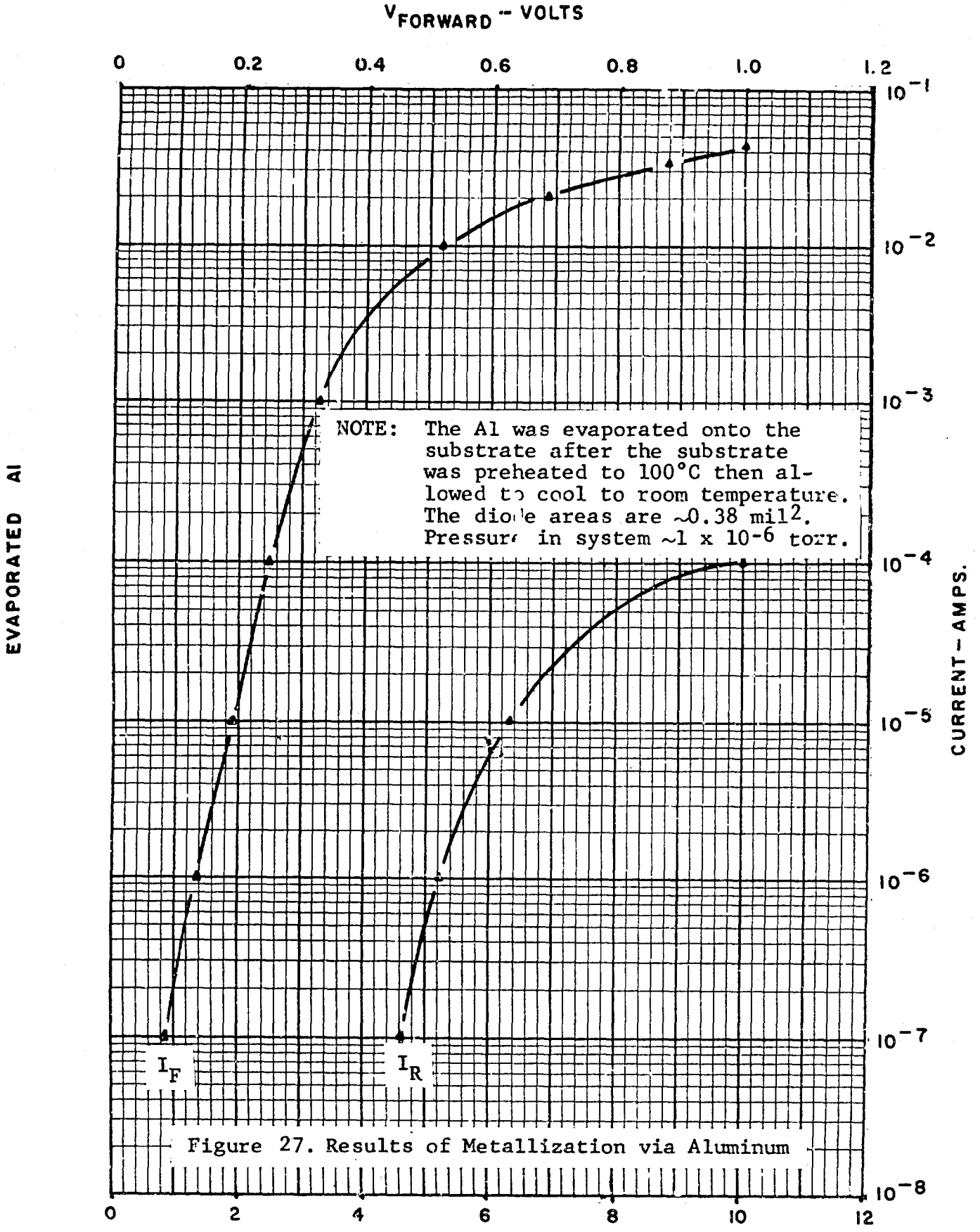

Figure 27. Results of Metallization via Aluminum

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Finally, an attempt was made to fabricate diodes using tungsten deposited by means of vapor plating.[3] This was very unsuccessful as can be seen in Figure 28. This characteristic is typical of what one sees when an oxide has been allowed to form on the silicon surface prior to the deposition of the metal. This has been encountered from time to time when a leak had developed in the sputtering system so that both air and argon were present. Thus, it appears that the atmosphere present during the plating process allowed a slight oxidation of the surface to take place. Further work with this technique might result in the elimination of this problem. But in view of the good results already achieved using the Mo-Au system, this will not be pursued on this contract.

4.4 CONTACT FORMING AND CREEP

It is well known that under the influence of the very large electric fields present in the vicinity of a metal-semiconductor contact, there may be a significant mobility of ions in this region. Thus, metal ions may be caused to drift across the barrier and into the semiconductor, and impurity ions themselves may move about within the barrier region.[4] In the former case, if the metal can act as either a donor or acceptor in the semiconductor, one can expect such migration to have pronounced effects upon the barrier shape, and hence, upon the observed characteristics of the diode, especially the current-voltage curve.

Thus, when choosing a contact metal, one has an additional consideration which is the effect the metal might have on the barrier profile should it migrate into the semiconductor. Evidence for such migration has been obtained in our laboratories, and the data shown in Figures 29 and 30 demonstrate the extent to which this effect is important.

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[3] C. F. Powell, J. H. Oxley, and J. M. Blocher, Vapor Deposition, John Wiley & Sons, New York, 1966.

[4] Heinz K. Henisch, Rectifying Semiconductor Contacts, Clarendon Press, 1957.

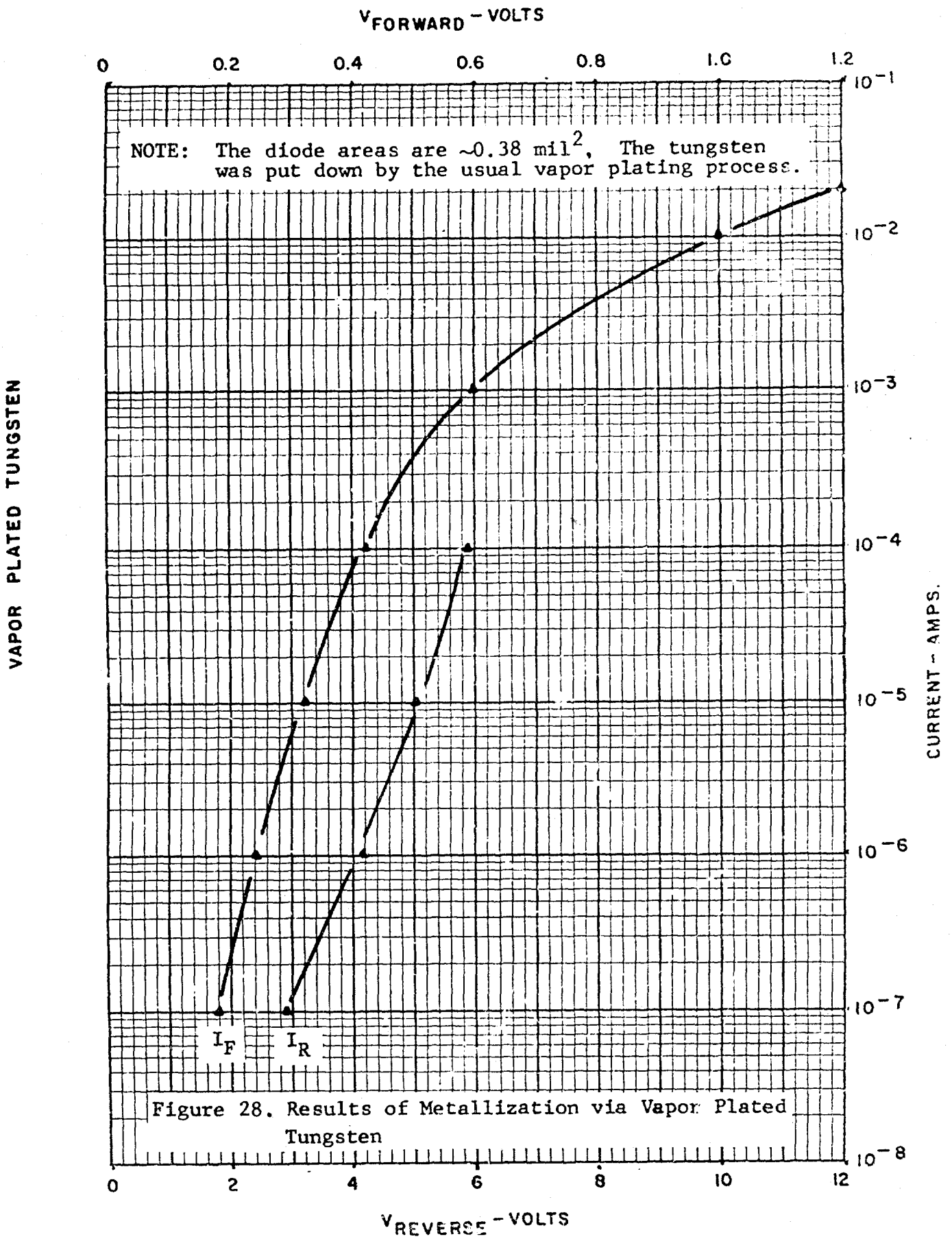

Figure 28. Results of Metallization via Vapor Plated Tungsten

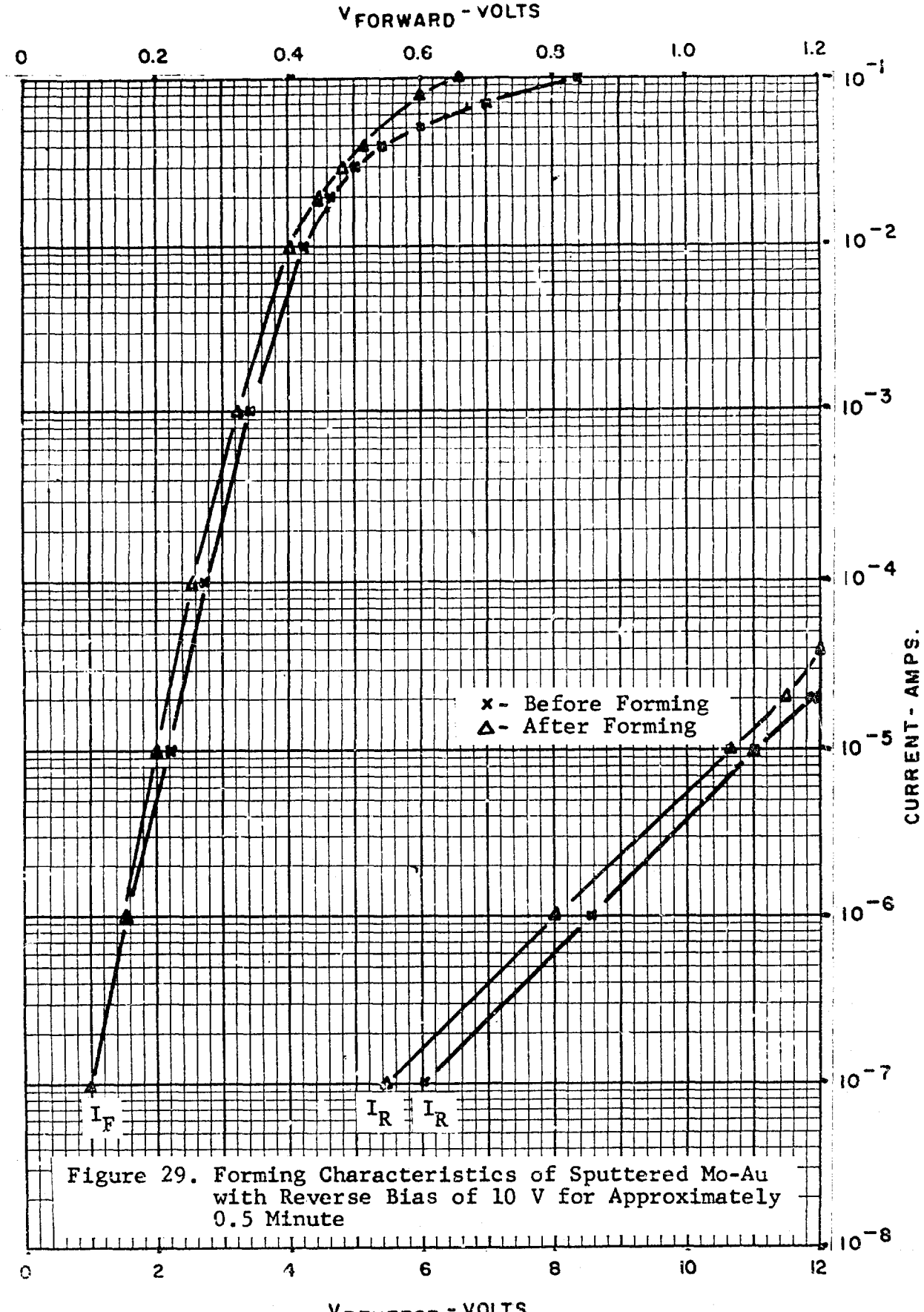

Figure 29. Forming Characteristics of Sputtered Mo-Au with Reverse Bias of 10 V for Approximately 0.5 Minute

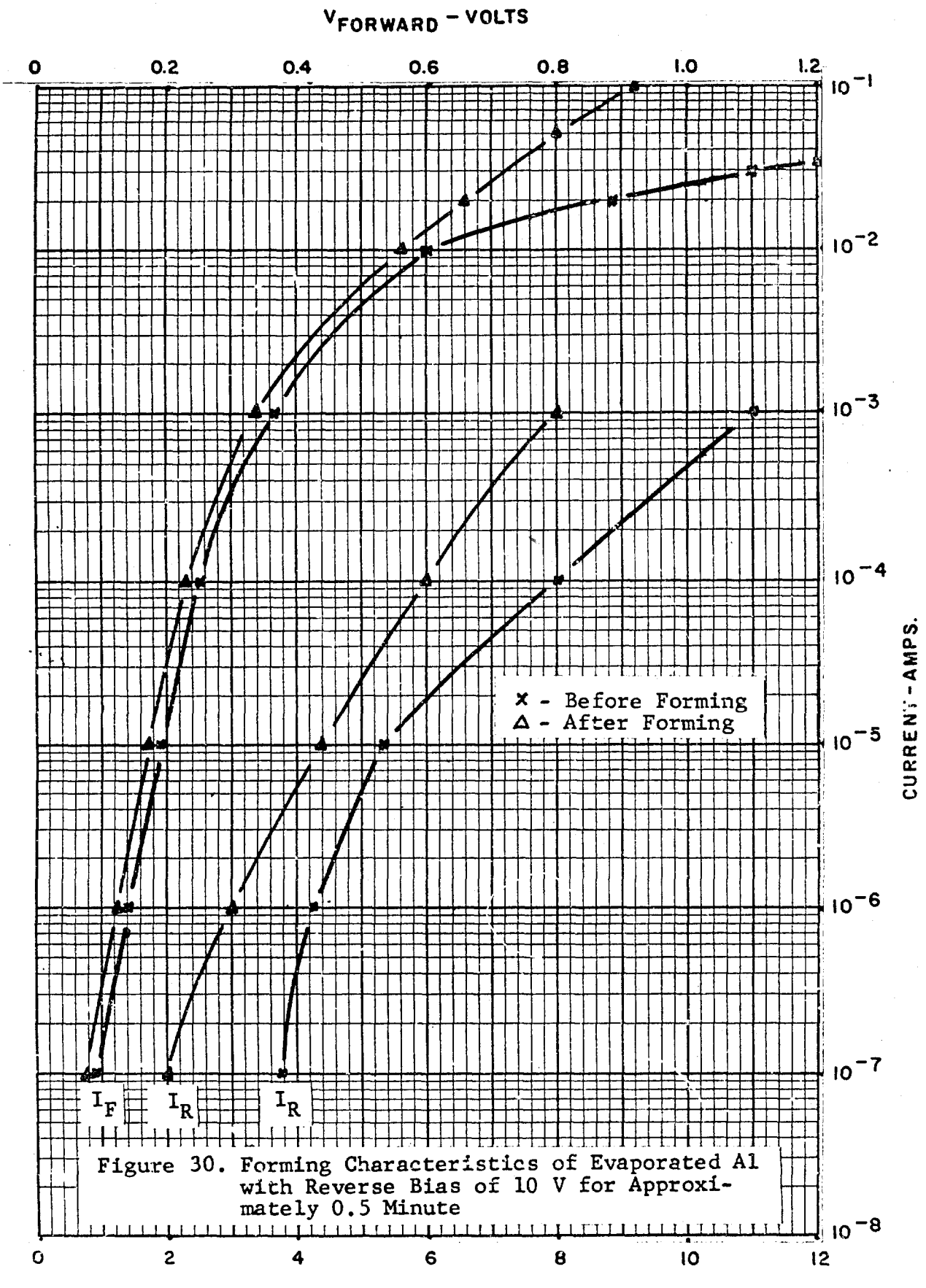

Figure 30. Forming Characteristics of Evaporated Al with Reverse Bias of 10 V for Approximately 0.5 Minute

In Figure 29 two current-voltage characteristics which were obtained on a single Mo-Au diode are shown. One of these was made prior to and the other after the application of a static reverse bias voltage of 10 volts for about 30 seconds. All of this was done at room temperature. The shift in the characteristic, though clearly visible, is not large enough to cause concern in this case. However, Figure 30 shows the results of the same treatment applied to an Al diode, and here the changes observed are dramatic.

It is to be expected that Al would be more troublesome in this regard since it acts as an acceptor in silicon and can radically alter the band structure in the vicinity of the contact.

Such forming experiments were also carried out on Cr diodes which showed changes slightly greater than that found with Mo, but the changes were still not great enough to make the diode unacceptable.

SECTION V

5.0 DIODE CHARACTERIZATION

5.1 INTRODUCTION

In Section 2 we introduced the equivalent circuit for the hot carrier diode and related the individual elements of this circuit to various parts of the actual diode for the purpose of analyzing loss mechanisms. Here, we describe how the elements of the equivalent circuit are determined from measurements made on the diodes and discuss the results of these measurements.

5.2 MEASUREMENTS

Three parameters are measured on a Tektronix 575 Curve Tracer. These are the reverse voltage at 10^{-5} ampere and the forward voltage drop at 50 and 100 mA respectively. The breakdown voltage is important because of its effect in limiting the output power achievable.

In the 50- to 100-mA region of the forward characteristic, the slope of the I vs V curve is generally constant so that the simple diode equation is not obeyed in this region. If one assumes that the barrier behaves like an ideal diode in series with a linear resistor, then the slope of the I vs V curve gives the value of this resistor in series with r_s, the resistance external to the barrier, so we have

$$R_F = R_b + r_s,$$

where:

$$R_F = \frac{V(100\ mA) - V(50\ mA)}{50\ mA}$$

At first it may seem strange to place an additional resistance, R_b, in the barrier region, but it must be kept in mind that we are dealing with current densities of the order of 4×10^4 A/cm^2 at these high current levels, and the behavior of a Schottky barrier under these conditions is likely to be quite different from the predictions of simple theory based upon low current density and low bias voltage.

The two forward voltage measurements at 50 and 100 mA yield another significant parameter for device evaluation. If the line drawn through these two points in the I-V plane is extrapolated back to the voltage axis, the point V_F is reached, where V_F is defined as

$$V_F = 2V(50\ mA) - V(100\ mA)$$

This voltage is a rough measure of the barrier height of the junction* and is also of direct importance in estimating the diode loss.

An illustration of the above measurements is provided by Figure 14 of Section 2.2 which shows the scope trace of the forward characteristic of a typical diode.

Figure 31 shows the test setup used for measuring the high frequency resistance of the device under resonant conditions. This is a small signal measurement and if the diode is at zero or negative dc bias, the high frequency current path through the device is via

*More accurate determinations of the barrier height have been made by means of capacitance and current density measurements. The parameter, V_F, is merely a convenient indication and a useful circuit concept.

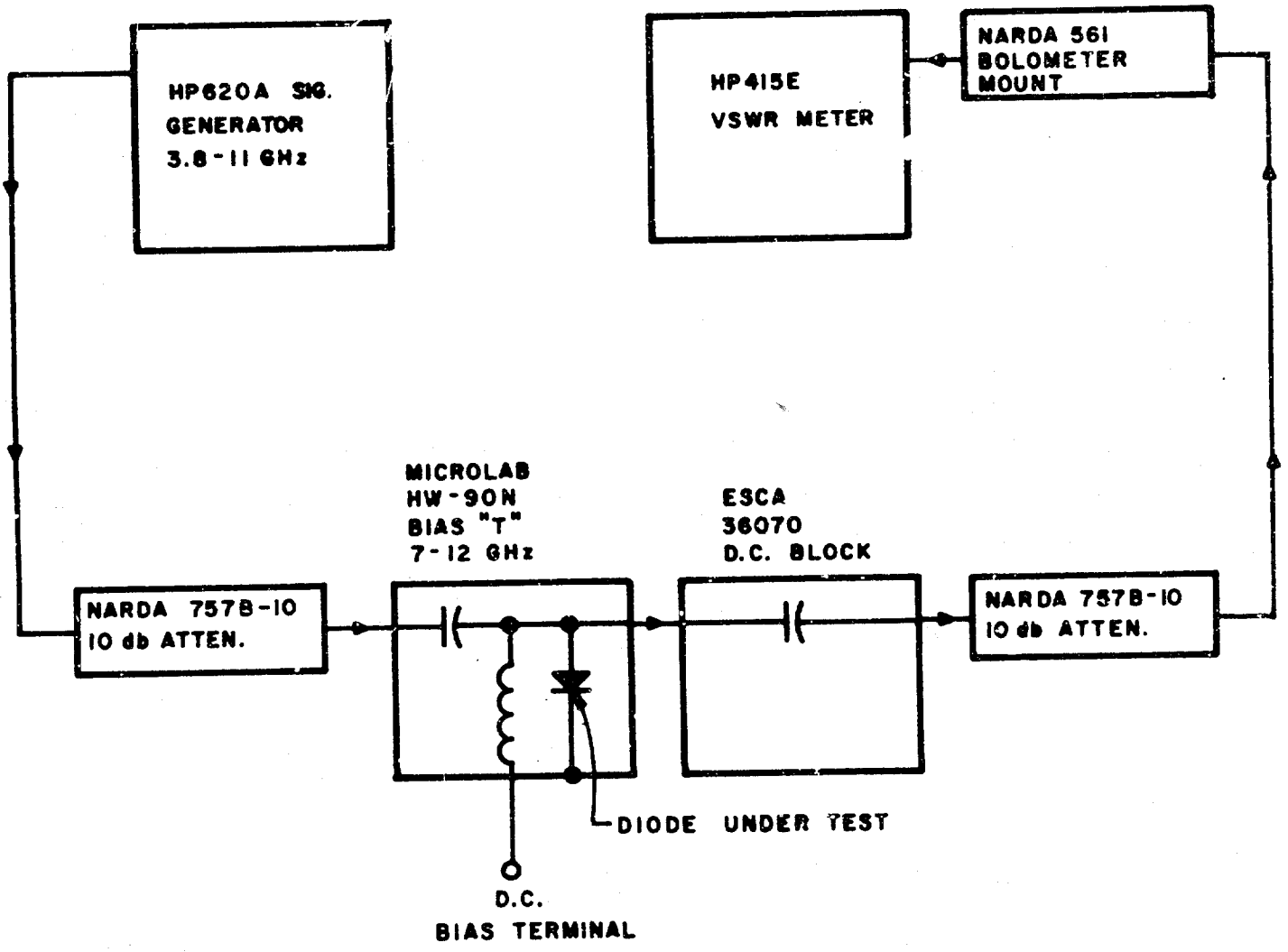

Figure 31. Measurement Setup for Determination of Resonant Frequency and Series Resistance of Hot Carrier Diodes

6035-2-7

L, r_s, and C_b. Thus, a frequency can be found where L and C_b are in series resonance and the resistance, r_s, may be measured directly by determining the power transmitted to a matched load shunted by the diode.

Finally, the capacitance of the diode is measured on a Boonton 75A, 1-MHz capacitance bridge. This figure is corrected for the case capacitance, measured directly on an open circuit package, to yield C_b.

5.3 EXPERIMENTAL RESULTS

Typical results of measurements made on a number of experimental hot carrier diodes having areas ranging from 0.2 to 5.0 mil^2 are summarized in Table II. Several features of this data are interesting.

First, noting that the parameter R_F consistently exceeds r_s, the high frequency resonant resistance, one is forced to the conclusion that the barrier resistance, R_b, must be substantial.

A second fact is brought out in Figure 32, which is a plot of $g_s = \frac{1}{r_s}$ and C_b as functions of the nominal device area. The capacitance behaves as it should increasing linearly with area. However, the high frequency conductance is not proportional to area and, in fact, saturates at a value of about 1.5 mhos, indicating a fixed loss of 0.66 ohm. If r_s were due entirely to spreading resistance, then g_s would vary as $A^{\frac{1}{2}}$ since the spreading resistance of a disc contact is given by

$$R = \frac{\rho}{4a} ,$$

TABLE II

VARIOUS DIODE PARAMETERS AS MEASURED ON DEVICES OF DIFFERENT AREAS

Device Number	$V_{Reverse}$ at 10^{-5} A	Cap.[1] at V = 0	r_s at Resonance	Resonant Frequency	R_F[2]	V_F[3]	Device Area[4]
	Volts	pF	Ohms	GHz	Ohms	Volts	Mil^2
D2	8.8	0.412	1.10	9.95	--	--	0.2
3	8.2	0.487	3.40	10.30	--	--	0.2
4	9.2	0.451	2.75	10.35	--	--	0.2
5	7.8	0.388	0.70	11.10	--	--	0.2
7	---	---	--	---	3.2	1.14	0.2
10	---	---	--	---	2.8	1.12	0.2
E2	10.4	0.536	0.93	9.87	5.6	0.84	0.4
3	8.2	0.556	0.80	9.20	--	--	0.4
4	8.6	0.581	0.80	9.20	5.0	0.70	0.4
5	5.1	0.535	1.50	8.90	5.2	0.64	0.4
6	8.0	0.475	1.25	9.70	6.0	0.74	0.4
F9	---	---	--	---	2.4	0.60	0.8
13	8.0	0.905	0.93	6.70	2.0	0.60	0.8
14	6.5	0.632	1.30	8.50	--	--	0.8
15	5.7	0.608	0.75	8.48	3.4	0.64	0.8
16	7.5	0.654	0.72	8.55	4.0	0.70	0.8
G2	8.0	1.30	1.00	5.80	1.4	0.53	1.6
3	8.0	1.15	1.10	6.40	1.6	0.53	1.6
4	8.1	1.41	0.95	5.60	1.4	0.56	1.6
5	7.5	1.26	0.82	6.10	1.4	0.54	1.6
H1	5.5	3.60	0.66	3.32	1.0	0.50	5.0
2	6.4	2.42	0.68	3.86	0.9	0.53	5.0
3	6.0	3.72	0.71	3.10	0.7	0.50	5.0
4	8.0	2.73	0.68	3.94	0.8	0.52	5.0

(1) This includes a case capacitance of 0.25 pF

(2) $R_F = \frac{V(100\ mA) - V(50\ mA)}{50\ mA}$

(3) V_F is the voltage axis intercept of the line drawn through the Points V (100 mA), I = 100 mA; V (50 mA), I = 50 mA, and is obtained from the formula, $V_F = 2V(50) - V(100)$

(4) This is the nominal area

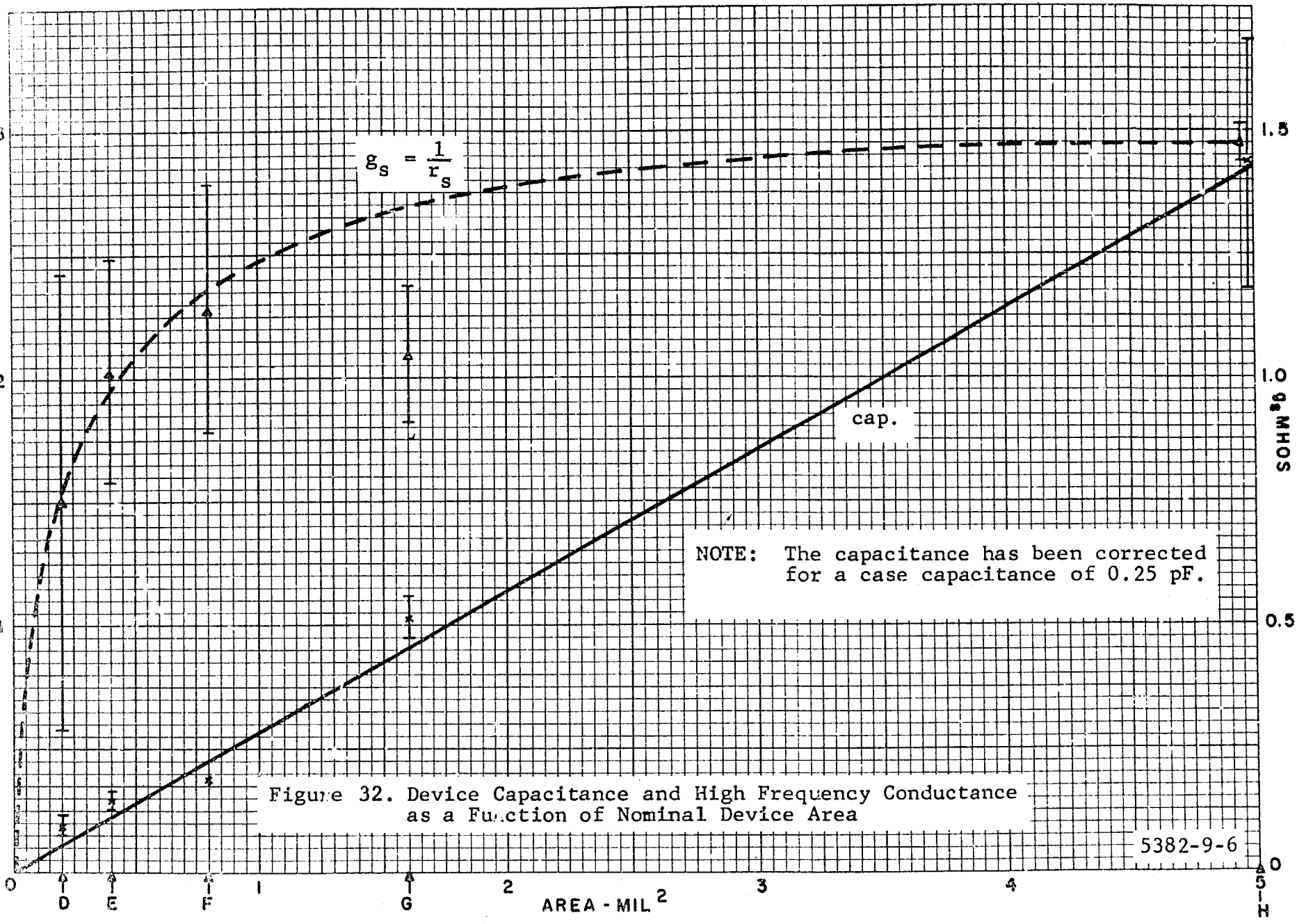

Figure 32. Device Capacitance and High Frequency Conductance as a Function of Nominal Device Area

where a is the contact radius. A simple attempt at curve fitting convinces one that the data of Figure 32 cannot be fitted by a square law dependence. Furthermore, a calculation of the resistance of a single gold wire 0.7 mil in diameter and 1/16 inch long at a frequency of 10 GHz, where the penetration depth is about 0.8 micron, yields a figure of 0.87 ohm. Our lead wire arrangement consists of four such wires in parallel so the minimum contribution due to these would be 0.22 ohm which accounts for 1/3 of the observed fixed resistance.

Actually, the geometrical arrangement of the four lead wires is such that a high frequency wave travelling down them would probably not utilize more than about half of the effective area; i.e., the area determined by the skin effect, so that the leads could account for most of the observed fixed resistance.

In view of the importance of the term, r_s, in contributing to losses in a rectifier circuit, it was felt worthwhile to try to design a different package that would further minimize the lead length of the bonding wire, or wires, to the die. Two attempts at this were made and these are described in the next subsection.

5.4 PACKAGE MODIFICATIONS

Figure 33 shows one approach to the problem of minimizing the series resistance of the package. The cone shaped electrodes are shaped so as to optimize the series inductance and shunt capacitance of the package, and contact to the diode active area is made via a silver button welded, or sintered, onto a silver-plated contact formed directly over the diode metallization.

Since only experimental quantities of these packages were to be fabricated the cost involved in special tooling for the end pieces and the ceramic tubes could not be justified for this contract.

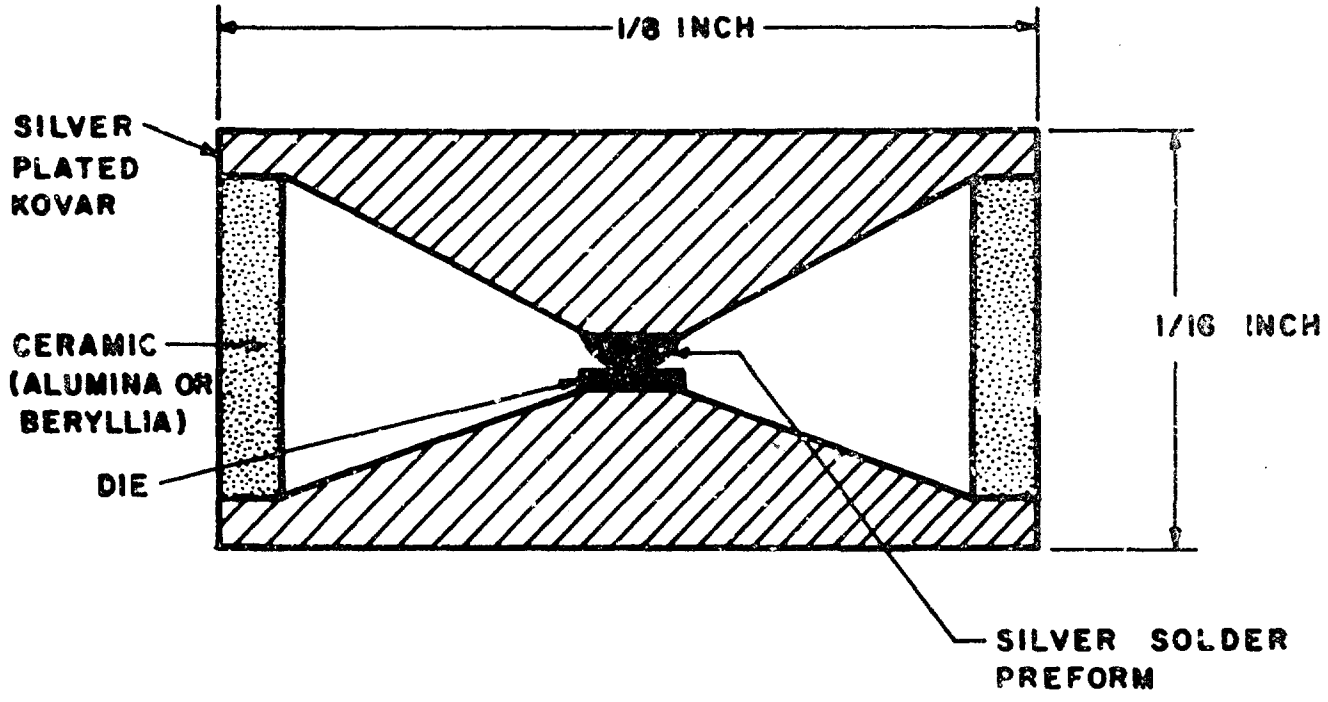

Figure 33. Experimental Diode Package

Hence, we attempted to make these pieces ourselves by turning the end caps out of Kovar and machining "green" alumina to size for the tubes, allowing for shrinkage during firing. Unfortunately, this process resulted in a very low yield, excessive wall thickness, and difficult tolerance problems.

A second approach to the problem is shown in Figure 34. This drawing shows a cross section of the standard "A" type pill package where the cap has been modified by drilling a small hole and depressing the center section toward the die so as to shorten the bonding wires.

A die for modifying the "A" package end caps as shown in Figure 34 was built and is shown in Figure 35. In Figure 36 a modified cap is pictured.

Numerous attempts were made to make successful wire bonds to both the cap and the die using these parts but it was finally concluded that this could only be done by suitably modifying one of our wire bonders so that the proper tension could be maintained in the 0.0007-inch gold wires. At this point it was decided that time did not permit the expenditure of further effort in this direction and this part of the project was terminated.

5.5 MINORITY CARRIER STORAGE LIFETIME

To estimate the loss contributed by storage effects, individual diodes were measured using the circuit shown in Figure 37. The method has been described in the proposal for this contract and is given in detail in the paper by Stewart M. Krakauer.[5]

[5] Stewart M. Krakauer, Proceedings of I.R.E., July, 1962, pp. 1674-1675.

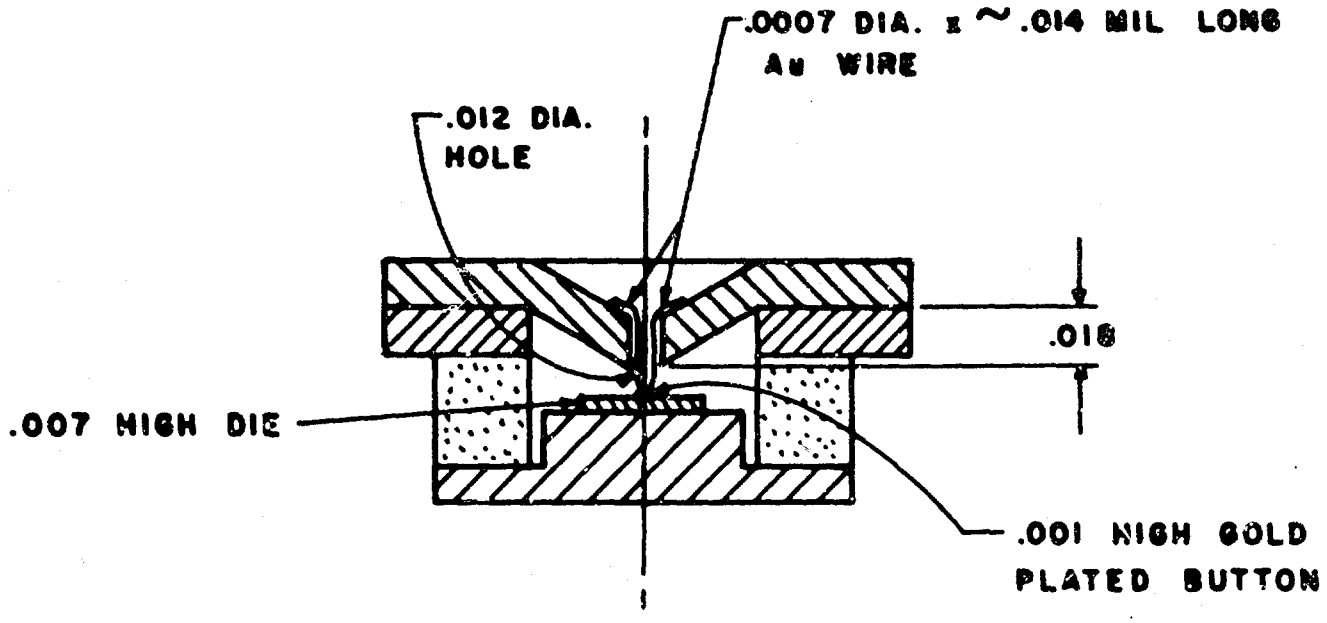

Figure 34. Schematic of Modified "A" Pill Package With Die Bonded to Pedestal and Wire Bonded to Cone-Shaped Electrode

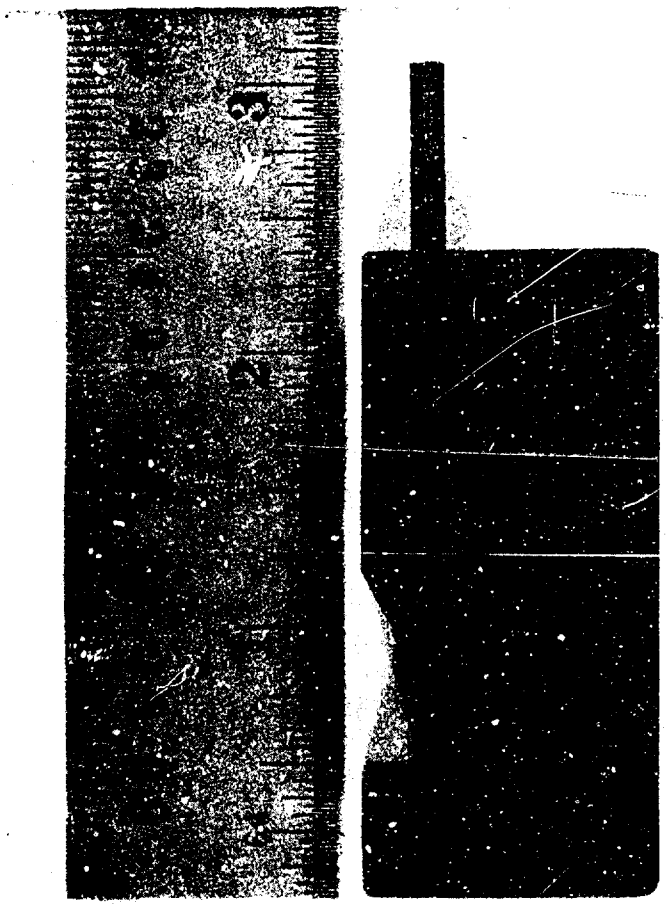

Figure 35. Die Used for Modification of "A" Pill Package Cap

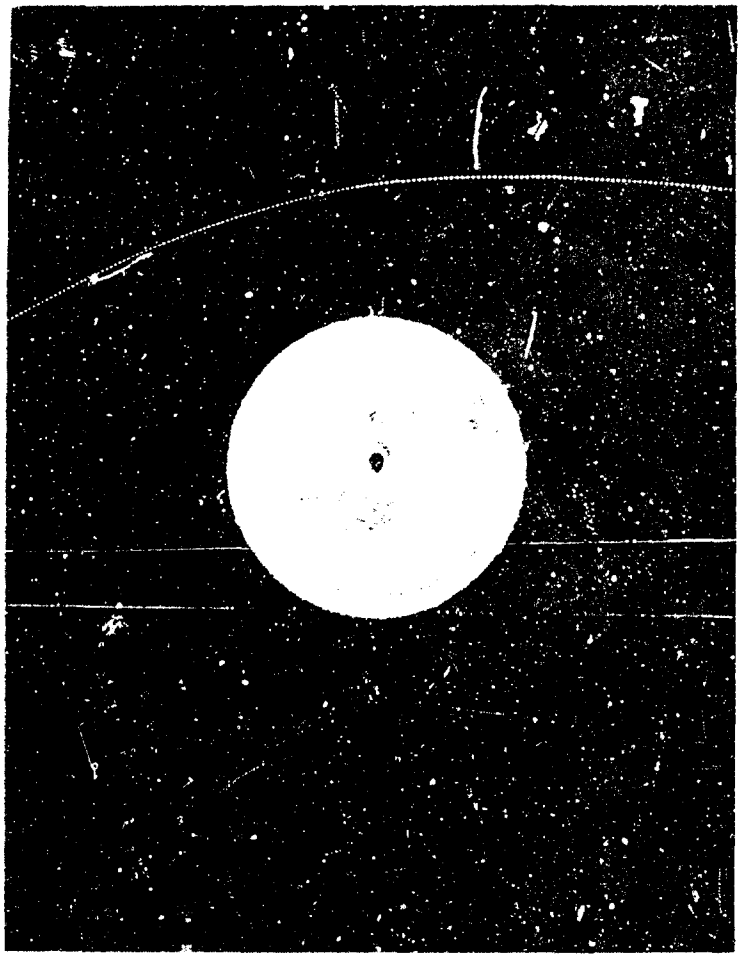

Figure 36. "A" Pill Package Cap After Modification with Die

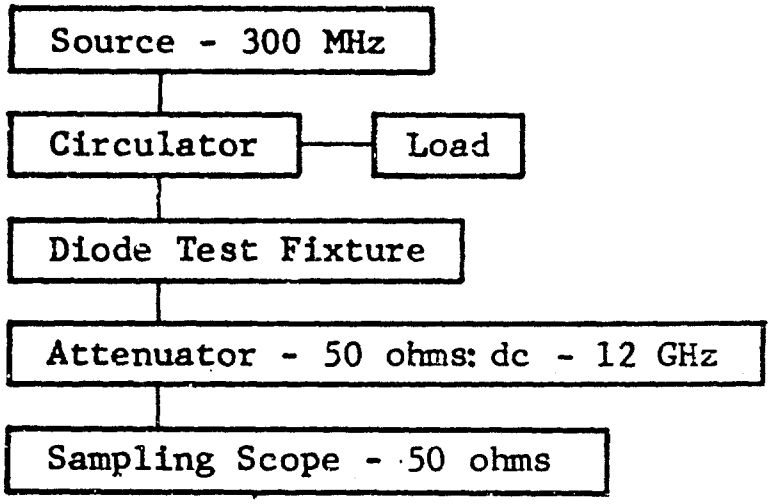

Figure 37. Lifetime Measurement Test Setup

Figure 38 shows the waveform expected from this circuit and Figure 39 shows typical diode waveforms actually obtained. Because the shape of these waveforms does not conform to the theoretical waveform, lifetimes are difficult to estimate. Basically, the measurement relates the reverse conduction angle (with a sinusoidal signal applied) to the lifetime of stored carriers. For small angles, the conduction angle and the peak amplitude are proportional. Thus, the lifetime of the carriers can be read as reverse current peak amplitude on a sampling scope. However, two phenomena are involved. Both stored charge and capacitance effects contribute to current. Ideally the two effects are separated by an abrupt change in slope. Waveforms that closely resemble the ideal trace shown in Figure 38 have been obtained with 120- to 150-ps lifetime diodes. When frequency was lowered with these 120-ps diodes, waveforms very similar to those shown in Figure 39 were obtained. It is therefore assumed that the nonideal waveforms are due to operation at too low a frequency and that a higher frequency would give clearer separation of stored charge and capacitive effects. If a conservative estimate is made, lifetime on these devices is less than 120 ps. This would be the value if it is assumed that all of the reverse current peak shown in Figure 39 was caused by charge storage effects. That this is a conservative assumption is indicated by the following: (1) the two waveforms shown in Figure 39 were obtained from devices on the same wafer identically processed, (2) the device used to obtain the waveform shown in Figure 39(a) had a capacity of about 3 pF; but for Figure 39(b) the device had a capacity of about 0.5 pF, (3) the higher capacity unit gave a larger reverse-current peak which shows that capacity significantly influences the reverse-current peak.

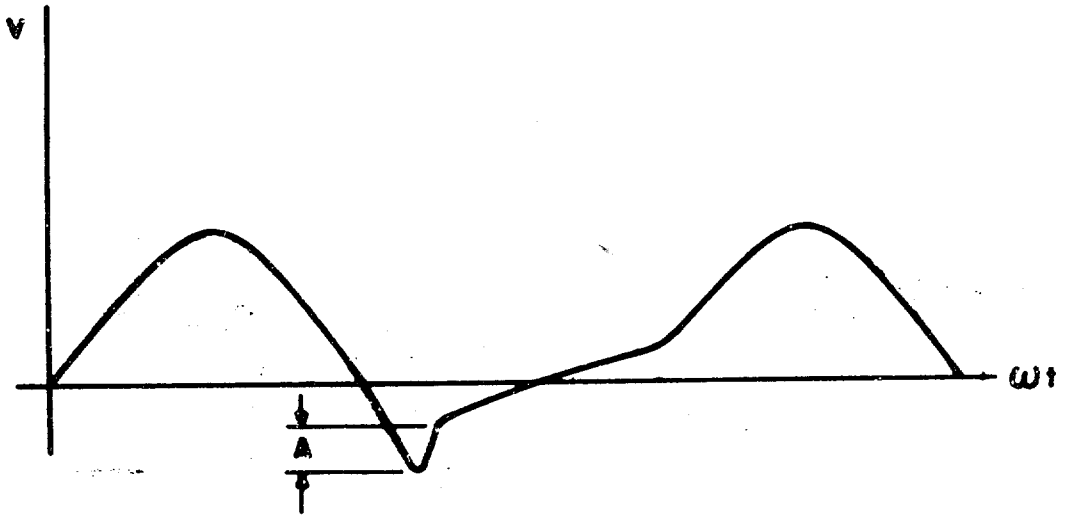

Figure 38. Waveform Obtained for High Lifetime Diodes (The applied signal is adjusted so that the amplitude of A indicates lifetime directly.)

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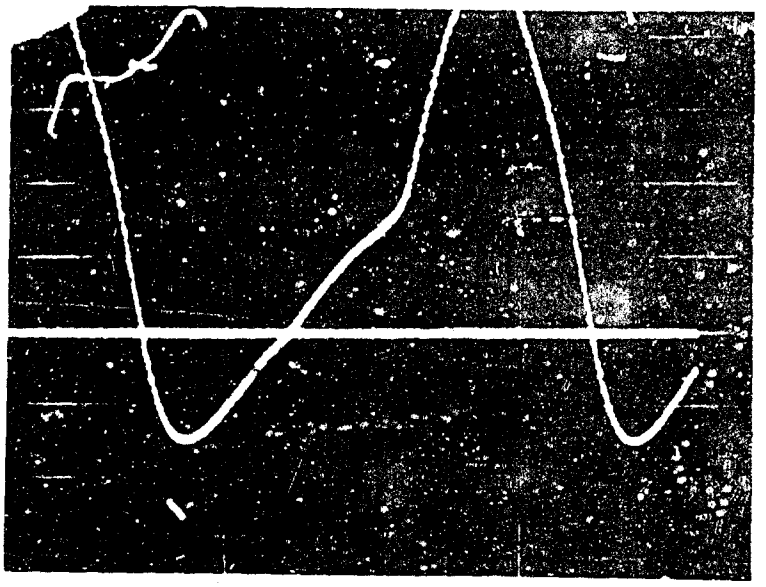
C = 3 pF

1 volt/cm

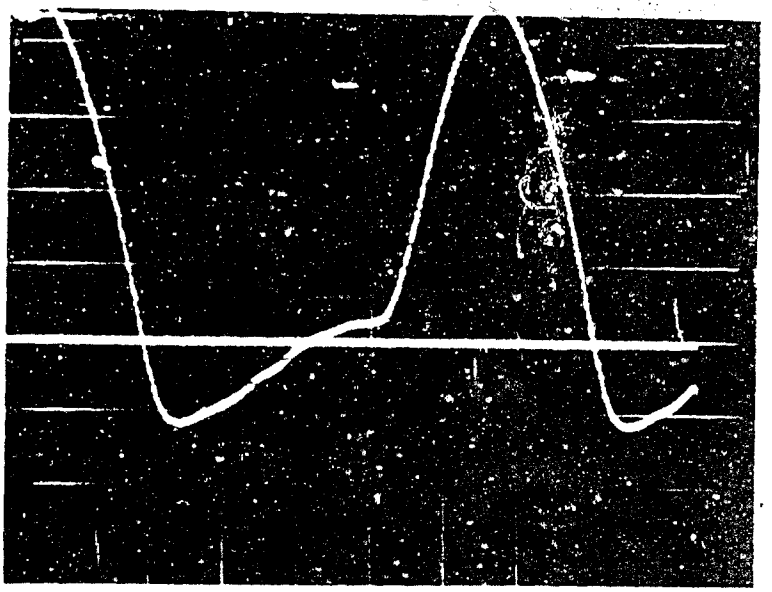


0.5 ns/cm (100 ps/cm)

(a)

C = 0.5 pF

1 volt/cm



0.5 ns/cm (100 ps/cm)

(b)

Figure 39. Waveforms Obtained for Lower Lifetime Hot Carrier Diodes

SECTION VI

6.0 LOW AND INTERMEDIATE FREQUENCY EFFICIENCY MEASUREMENTS

6.1 INTRODUCTION

In an effort to verify some of the conclusions drawn on the basis of the analysis presented in the first part of this report and to provide further insight into the operation of various rectifier circuits, measurements were made on rectifiers operating at low frequency (1 kHz) and at intermediate frequencies (15 to 100 MHz).

These measurements are described in this section.

6.2 LOW FREQUENCY MEASUREMENTS

To check the validity of the ideal analysis, measurements were made on a full-wave bridge-rectifier test circuit with a capacitor output filter. The circuit was designed to be as close as possible to the ideal of Figure 2. To this end, the frequency of operation was kept at 1 kHz so that parasitics in the diodes were negligible. The diodes chosen had low capacitance, high breakdown voltage (>50 volts), and low forward voltage drop (~0.3 volt).

Figure 40 shows a block diagram of the components used for the test. Figure 41 is a plot of the efficiency as a function of input power.

For nearly matched conditions, the efficiency asymptotically approaches 92 percent as it should according to theory. In fact, at P_{in} = 85 mW, the diode loss was computed from oscillographs of the diode current and voltage to be about 2 percent, bringing the agreement well within experimental error.

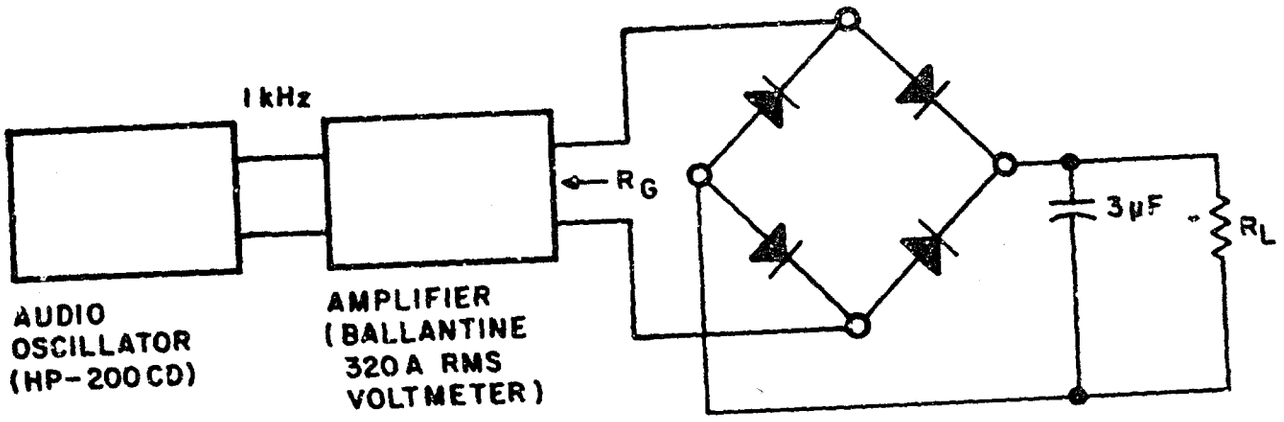


Figure 40. Diagram of Low-Frequency Full-Wave Capacitor-Output Bridge Rectifier Test Circuit

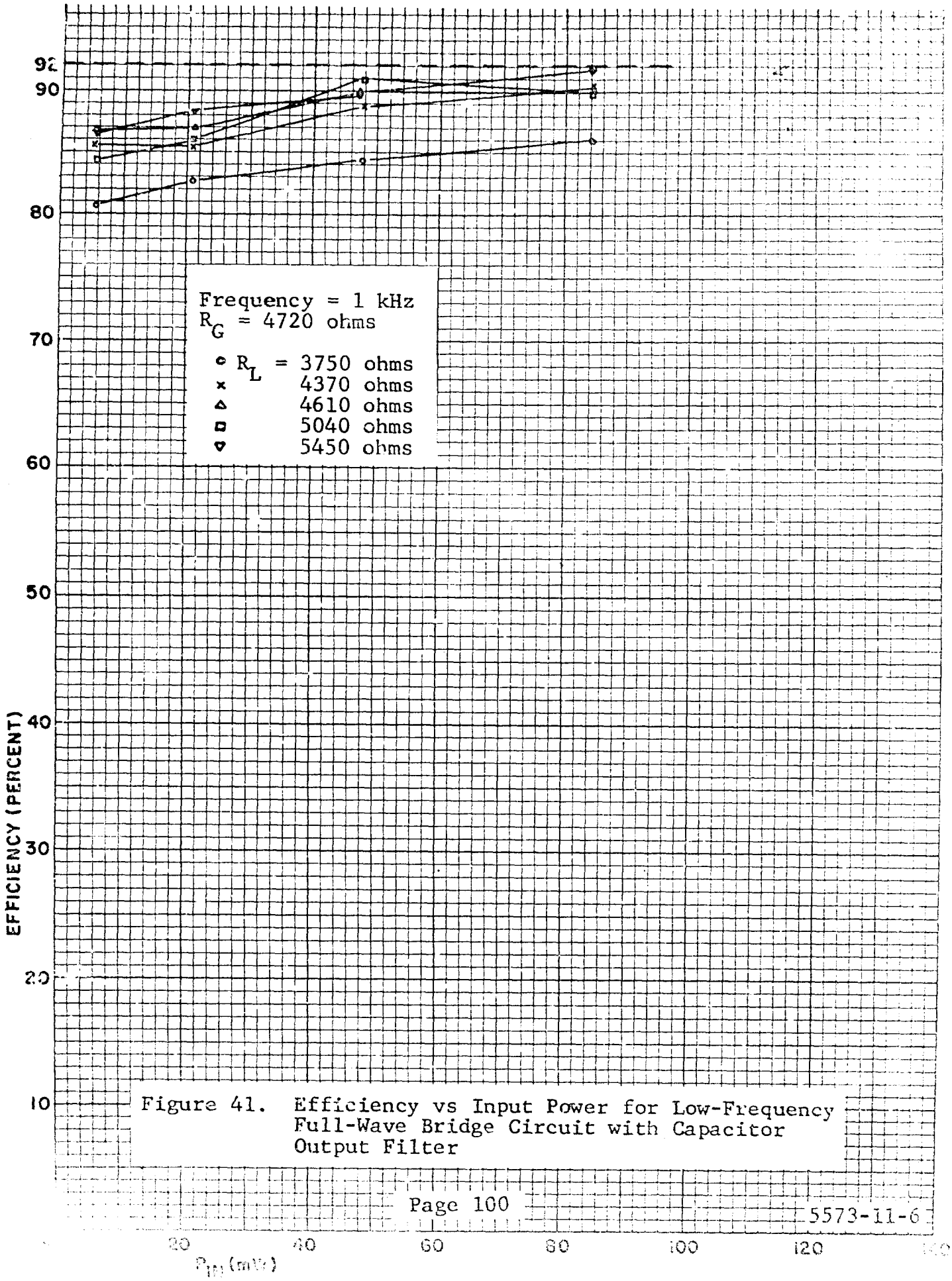


Figure 41. Efficiency vs Input Power for Low-Frequency Full-Wave Bridge Circuit with Capacitor Output Filter

Finally, the bridge-current and input-voltage waveforms in Figure 42 show again that the agreement with the predictions of Figure 2 is excellent.

6.3 INTERMEDIATE FREQUENCY MEASUREMENTS

To determine the effect of a shunt tuned input filter on the operation of the full-wave bridge, the circuits of Figures 43(a) and 43(b) were used.

The efficiency data obtained at frequencies of 15, 20, 25, and 30 MHz are tabulated in Tables III and IV and plotted graphically as a function of input (available) power in Figures 44 and 45 for the unfiltered and filtered input circuits, respectively.

No clear-cut inferences can be drawn from this data as the filter does not appear to result in an improvement in efficiency. Examination of the actual waveforms obtained for the unfiltered and filtered cases, shown in Figures 46 and 47, reveals a behavior in general agreement with the results of analysis, as can be seen by comparing Figure 47(a) with Figure 9(c), of Section 1.4.2.

Figure 47(b) demonstrates the effect of a slight detuning of the input filter on the phase relationship between the current waveform and the source voltage, e. Such detuning is accompanied by a substantial reduction in efficiency.

It is possible that the accumulation of Q losses in the input circuit is responsible for the lack of improvement with the filter. While this circuit is an excellent vehicle for studying the rectification process at tens of megahertz, it was not felt worthwhile to pursue such matters as the above discrepancy at this frequency since the situation is so far removed from that prevailing at the frequencies of ultimate interest, i.e., in the microwave region. Hence, no further work was done at these frequencies.

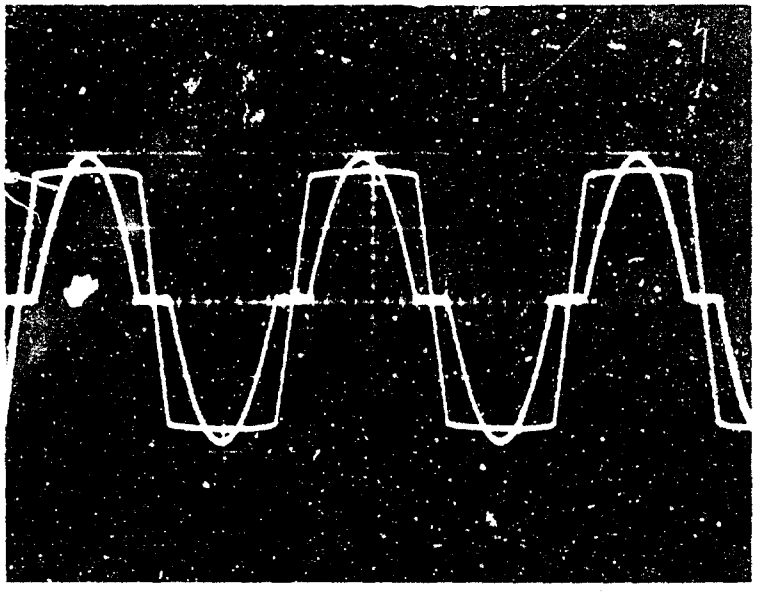
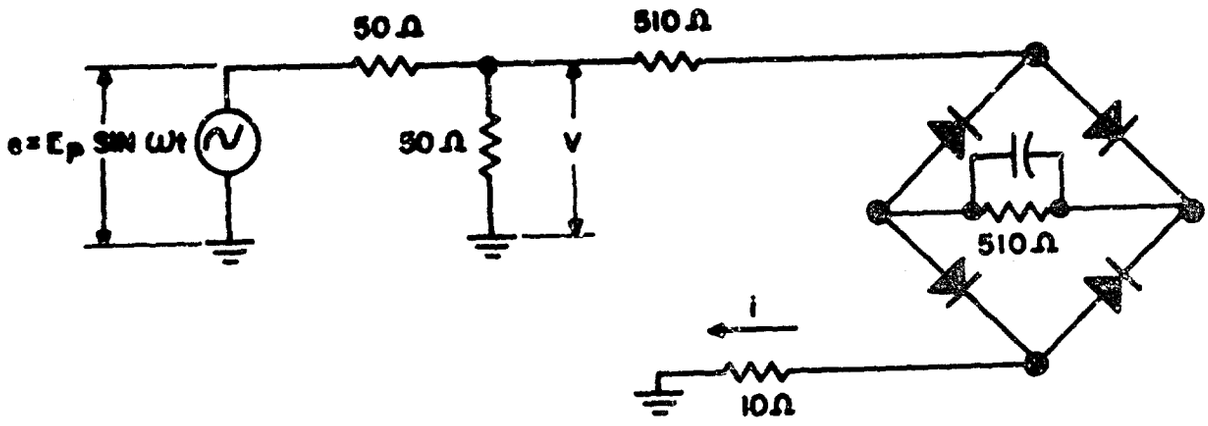
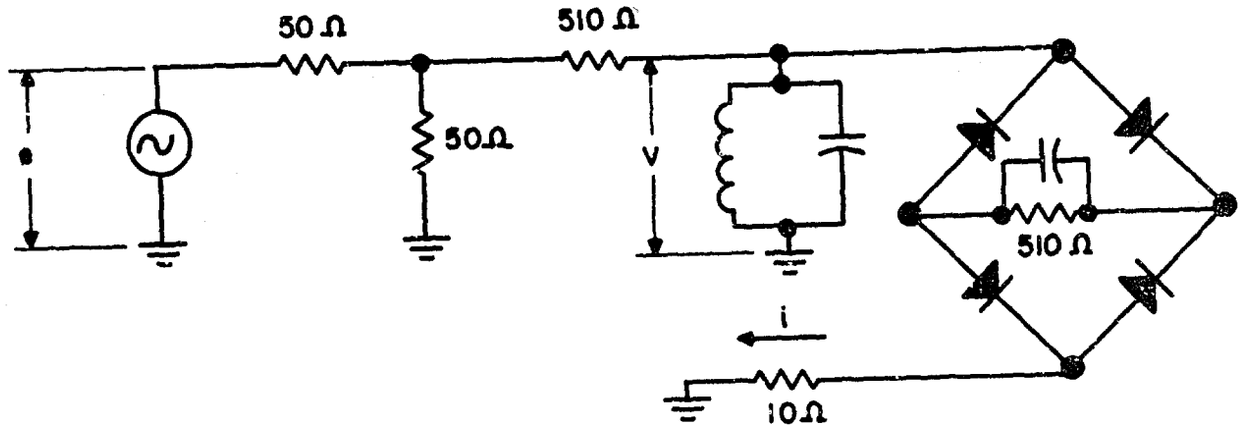


Figure 42. Input Current and Voltage Waveforms as Measured on Low Frequency Full-Wave Bridge Circuit with Capacitor Output Filter



(a) Without Input Filter



(b) With Shunt Input Filter

Figure 43. Circuit Diagram Efficiency Measurements on Full-Wave Bridge Rectifier

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TABLE III

EFFICIENCY VS POWER AVAILABLE

FULL-WAVE BRIDGE WITHOUT FILTER

Power Available (mW)	Frequency (MHz)	η = Efficiency (%)
90	15	86.8
55	15	84.5
24.6	15	75.3
6.1	15	53.2
90	20	84.8
55	20	77.6
24.6	20	72.8
6.1	20	53.2
90	25	81.5
55	25	78.3
24.6	25	70.5
6.1	25	49.2
90	30	81
55	30	77.4
24.6	30	72.8
6.1	30	53.2
90	35	81.5
55	35	75
24.6	35	70.5
6.1	35	49.2

TABLE IV

EFFICIENCY (η) VS POWER AVAILABLE

FULL-WAVE BRIDGE WITH FILTER

Power Available (mW)	Frequency (MHz)	η = Efficiency (%)
90	15	82.8
55	15	80.8
24.6	15	72.8
6.1	15	54
90	20	82.4
55	20	79.5
24.6	20	72.8
6.1	20	54.7
90	25	81.5
55	25	78.5
24.6	25	71.5
6.1	25	50
90	30	82.4
55	30	79
24.6	30	74
6.1	30	57.4
90	35	84.8
55	35	79
24.6	35	72.8
6.1	35	55.7

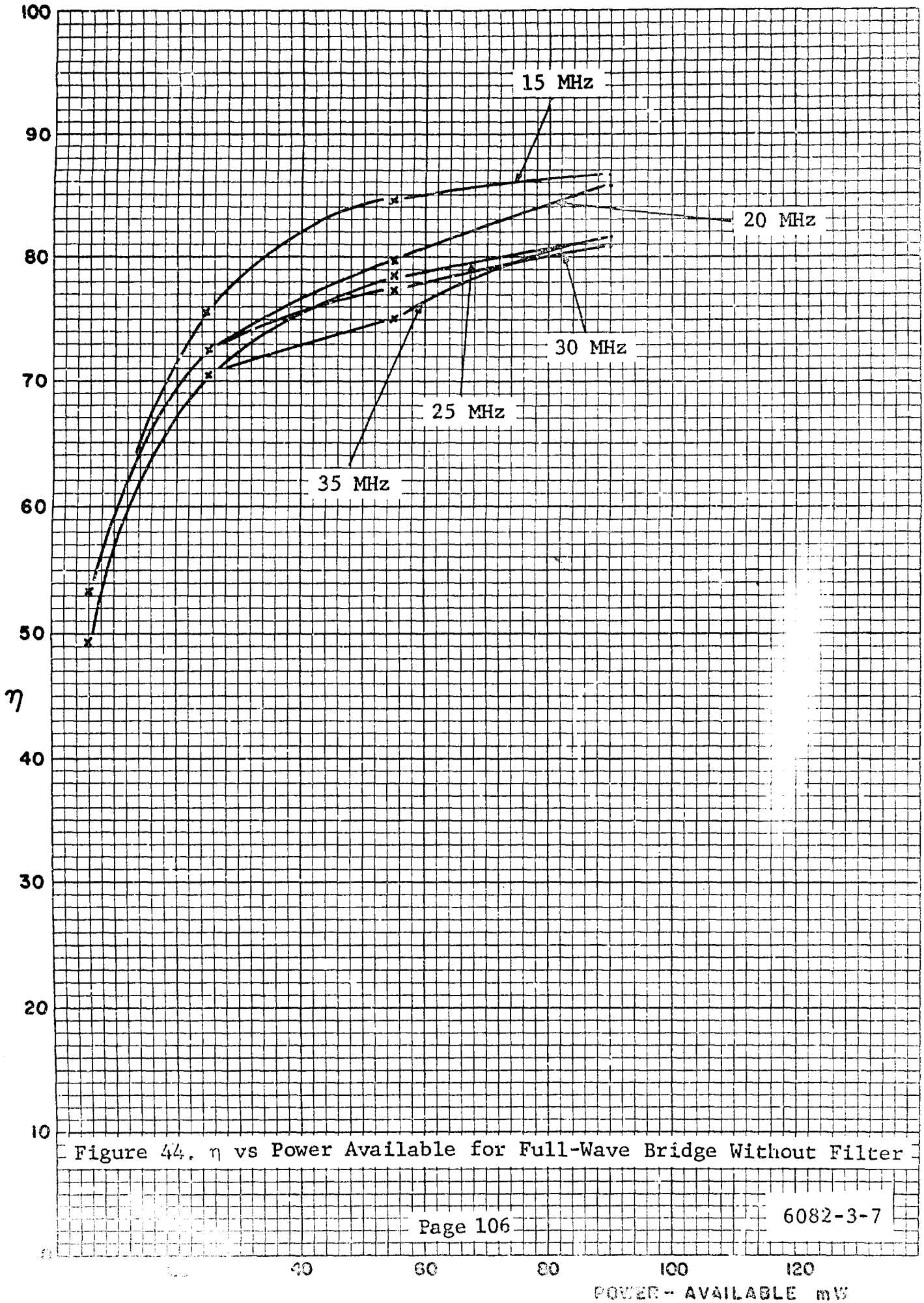

Figure 44. η vs Power Available for Full-Wave Bridge Without Filter

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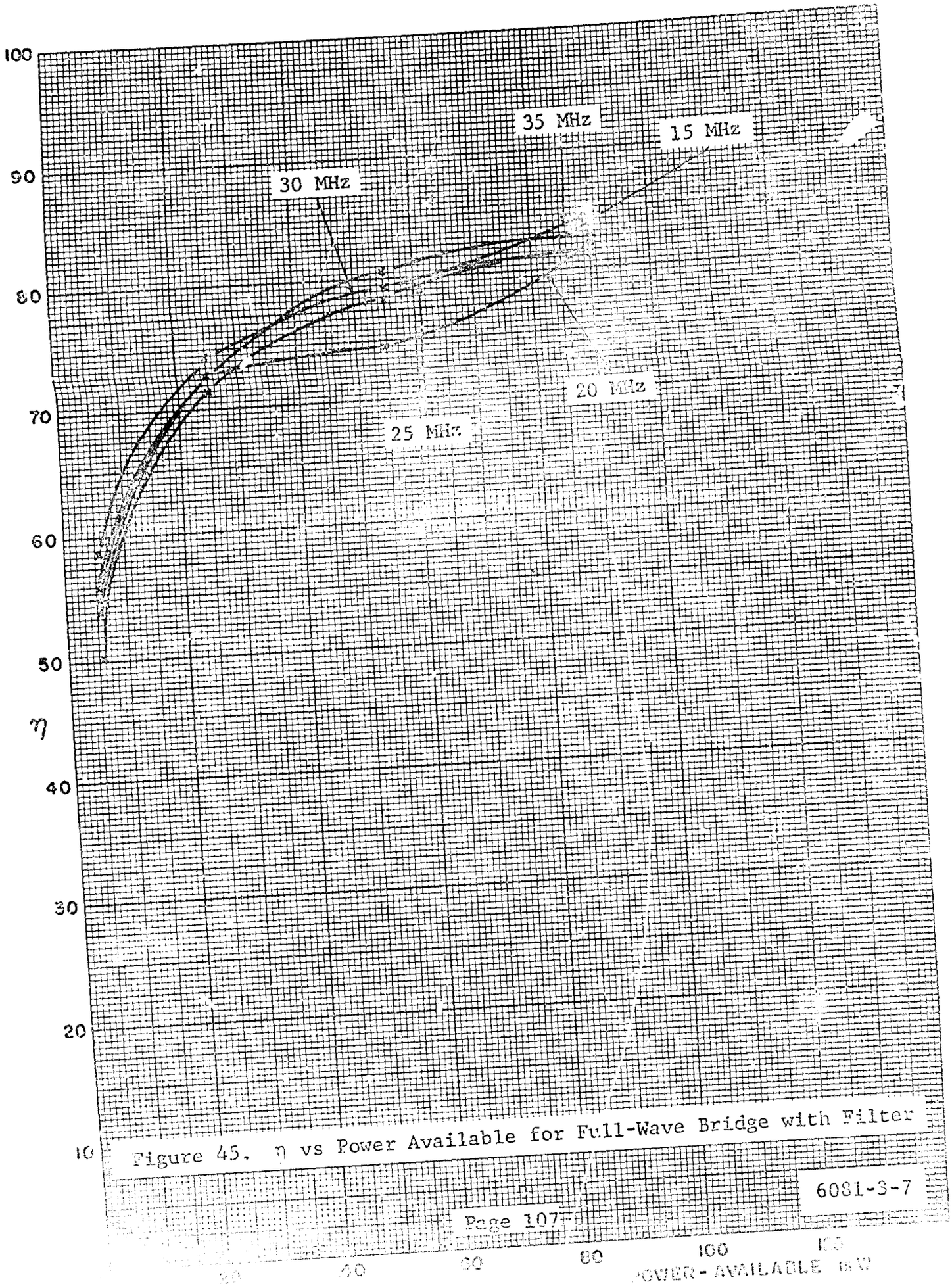

Figure 45. η vs Power Available for Full-Wave Bridge with Filter

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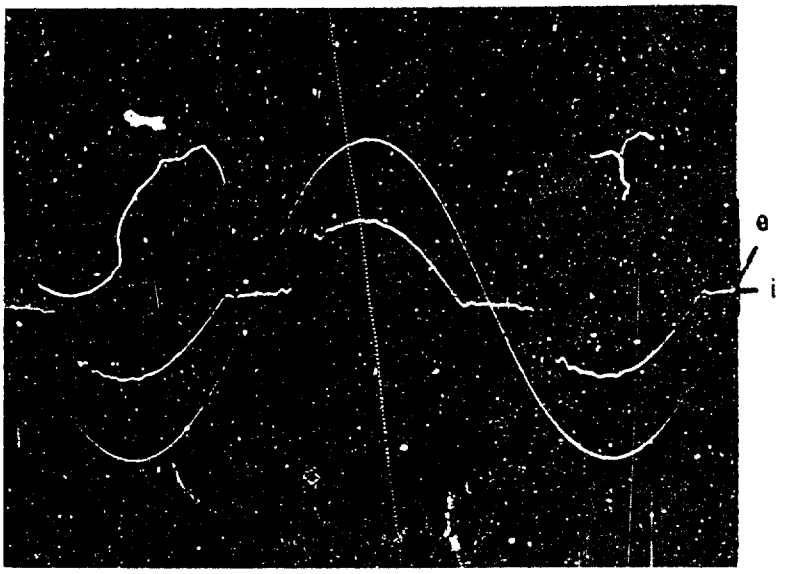
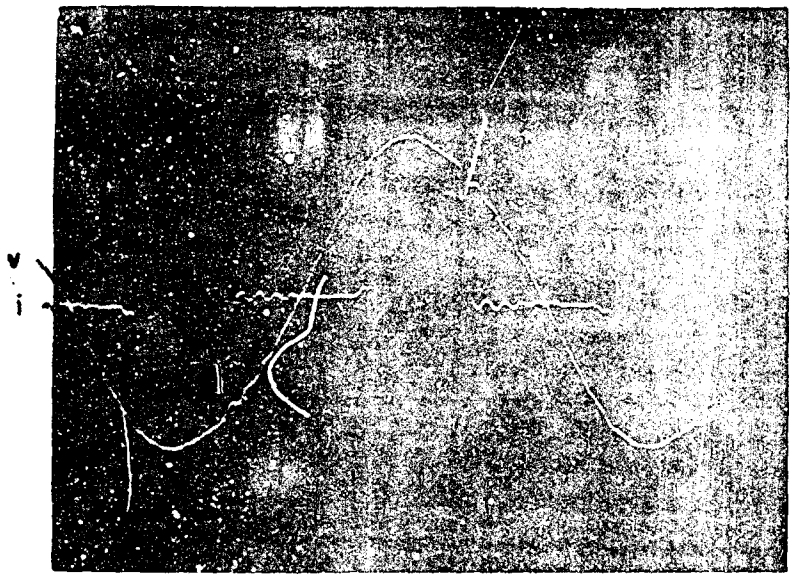


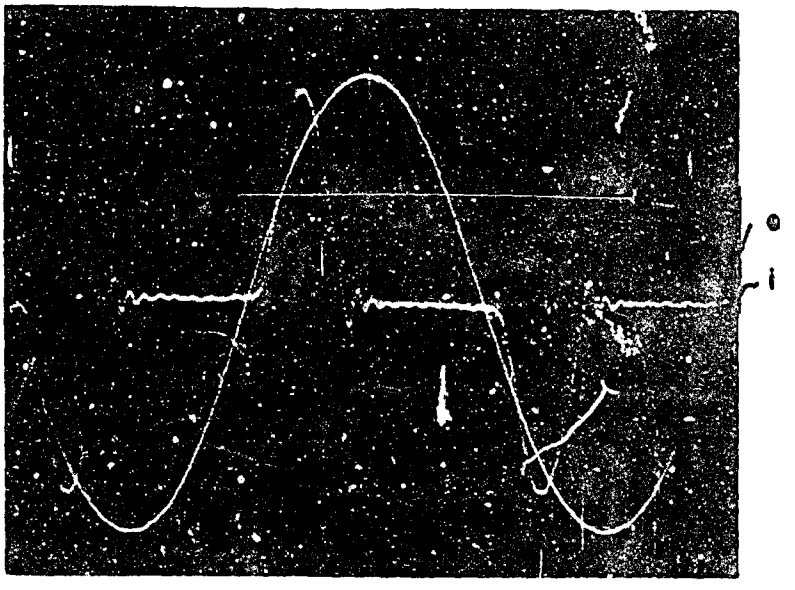
(a) e and i waveform

(b) v and i waveform

Figure 46. Waveforms for Full-Wave Bridge without Filter



(a) v and i in phase; max η obtained



(b) e and i out of phase; filter detuned

Figure 47. Waveforms for Full-Wave Bridge with Filter

One further experiment was carried out at a frequency of 100 MHz using a half-wave circuit with shunt input tuning. The source impedance for this circuit was 50 ohms, and the data are shown in Table V and Figure 48. These results closely resemble those obtained in the microwave range, and described in Section 7.

TABLE V

EFFICIENCY MEASUREMENTS ON HALF-WAVE CIRCUIT

Frequency Setting 100 MHz

R_L Ω	P_{in} Watt	V_{DC} Volt	η %	R_L -Ω	P_{in} Watt	V_{DC} Volts	η %	R_L -Ω	P_{in} Watt	V_{DC} Volts	η %
50	0.1	1.72	58.5	75	0.1	2.13	60.5	100	0.1	2.39	57
50	0.2	2.6	67.5	75	0.2	3.21	68.7	100	0.2	3.58	64
50	0.3	3.275	71.4	75	0.3	4.04	72.5	100	0.3	4.49	67.2
50	0.4	3.84	73	75	0.4	4.71	74.3	100	0.4	5.24	68.5
50	0.5	4.33	75	75	0.5	5.31	75.5	100	0.5	5.91	70.5
50	0.6	4.79	76.4	75	0.6	5.88	77	100	0.6	6.39	68.2
50	0.7	5.195	77.5	75	0.7	6.32	76	100	0.7	6.69	64
50	0.8	5.59	78	75	0.8	6.60	72.5	100	0.8	6.93	59.3
50	0.9	5.90	77.4								
50	1.0	6.13	75								

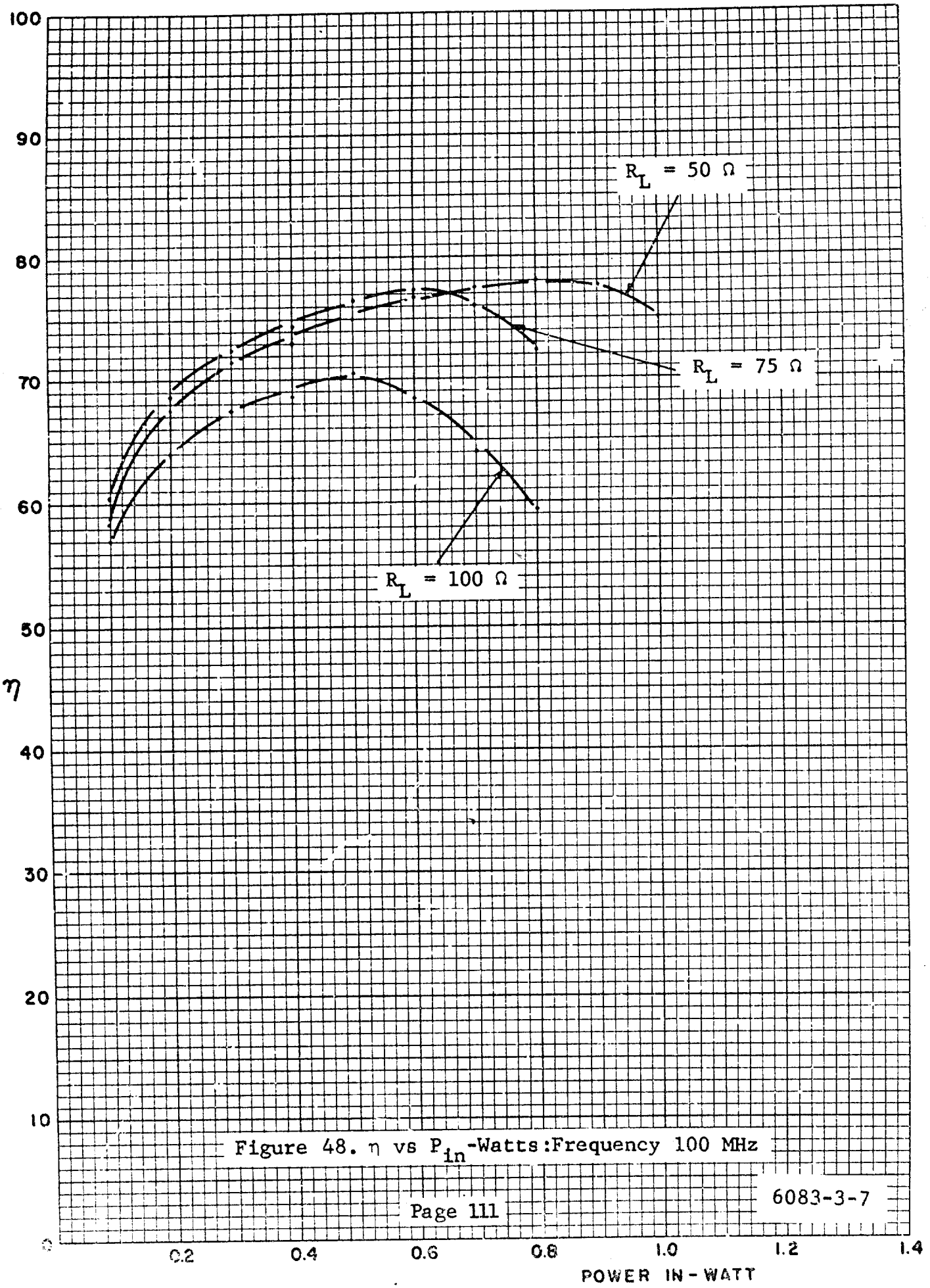


Figure 48. η vs P_{in}-Watts:Frequency 100 MHz

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SECTION VII

7.0 EFFICIENCY MEASUREMENTS AT MICROWAVE FREQUENCIES

7.1 INTRODUCTION

We now proceed to describe the microwave measurements carried out on the hot carrier diodes fabricated during the contract period. Three basic configurations have been studied and these will be described in turn. First, full-wave bridge circuits were constructed in waveguide for operation at 4 and 8 GHz. Next, a half-wave circuit was constructed using 50-ohm coaxial cable, and finally some experiments were performed using stripline techniques, where full-wave balanced circuits were studied.

7.2 MEASUREMENT CIRCUIT AND PROCEDURE

Figure 49 is a schematic diagram of the test equipment setup used in the measurement of rectification efficiency. Basically, it consists of a signal generator-power amplifier combination followed by a ferrite circulator, a narrow band filter, two directional couplers, a double-stub tuner, and finally, the rectifier. While a bridge rectifier is shown, essentially the same test circuit is used for all rectifier efficiency measurements.

The directional coupler nearest to the rectifier diverts approximately 1 percent of the incident power into a thermistor mount which then gives a direct measure of the input power to the rectifier. The remaining coupler samples 1 percent of the reflected power and provides a measure of the match being achieved. The double-stub tuner serves as a means for matching into the rectifier, which, in general, does not present a 50-ohm load impedance to the source.

A photograph of the equipment is shown in Figure 50.

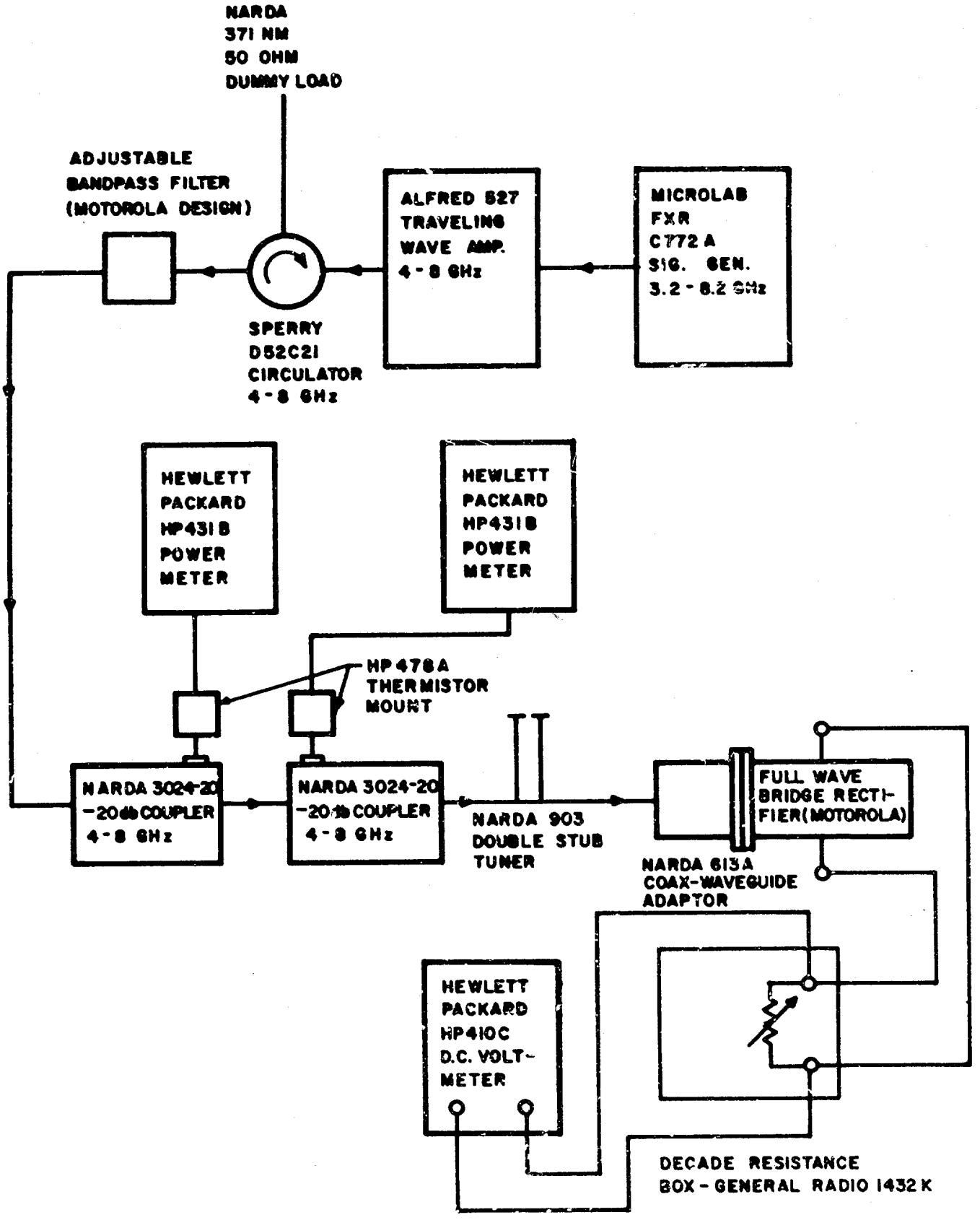


Figure 49. Efficiency Measurement Test Setup--
Schematic Diagram

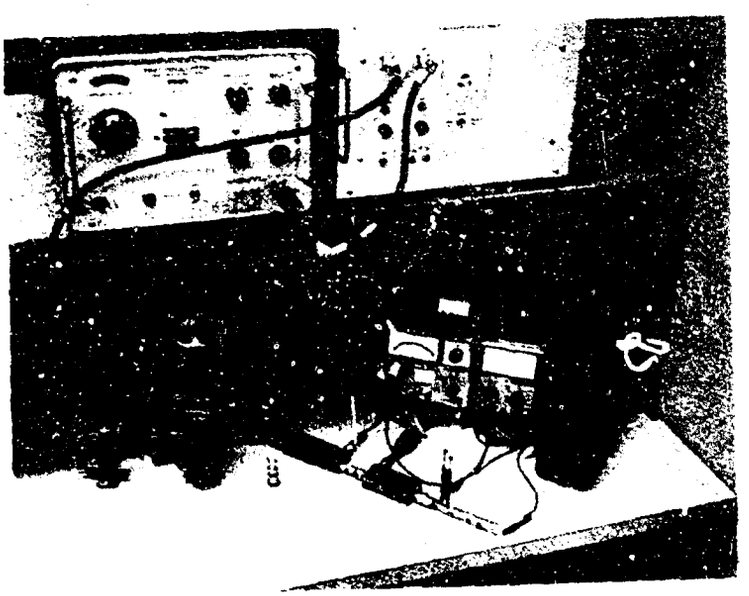


Figure 50. Photograph of Test Equipment Setup for Measuring AC-DC Conversion Efficiency in the Frequency Range 4-8 GHz. Two Full-Wave Bridge Rectifiers are Shown Together with a Single Diode Test Fixture

The measurements are carried out as follows: With the rectifier in place, the input power is slowly increased until a reading of about 50 mW is obtained on the incident power meter. At this point, the reflected power meter will usually show a substantial reading and preliminary tuning is carried out with the double-stub tuner to minimize this. The power is then adjusted again until a 50-mW input level is reached and the procedure is repeated. This procedure is repeated until the reflected signal is less than 1 percent of the incident reading, at which time a final adjustment of the input power is made.

This final input power reading is corrected for the exact coupling factor of the incident power directional coupler, and the previously measured insertion loss of the double stub tuner.

There is some uncertainty in this latter correction as the insertion loss of the tuner depends upon the degree of mismatch that is being tuned out by the stubs. For example, measurements have shown that when the tuner is terminated so that a VSWR of nearly 1.0 is present, the insertion loss is approximately 0.1 dB, while for a VSWR of 4.0 the insertion loss is 0.36 dB. Since it is inconvenient to measure this loss for each measurement condition we have used a standard correction of 0.1 dB for all rectifier efficiency measurements. Thus, our data represents a lower limit to the true efficiency in each case.

7.3 FULL-WAVE BRIDGE RECTIFIER

Figures 51 and 52 show the 4-GHz full-wave bridge rectifier. It is constructed from RG-49/U waveguide with the four diodes held in place by means of brass screws through the broad faces of the guide. These secure the diodes to two brass posts which enter through the short faces and are insulated from the

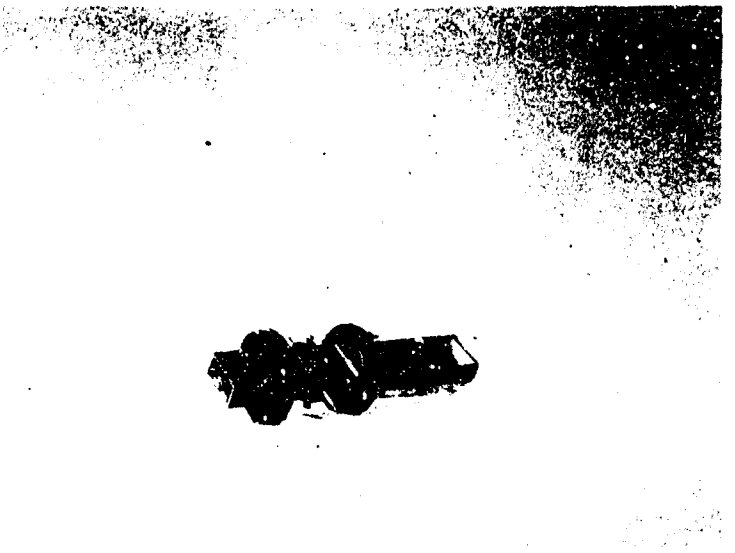


Figure 51. Photograph of Full-Wave Bridge Rectifier Fabricated in RG49/U Waveguide, Showing Coax-Waveguide Coupler and Adjustable Short

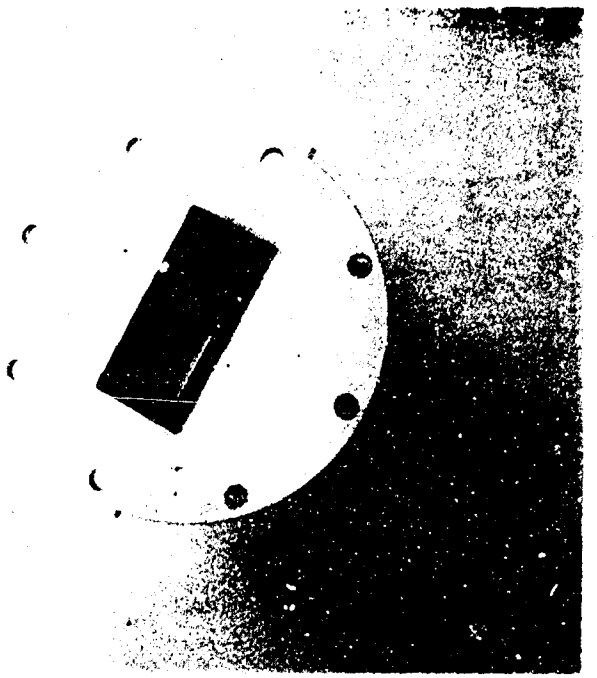


Figure 52. Photograph of Full-Wave Bridge Rectifier Fabricated in RG49/U Waveguide, Showing Method of Mounting Hot Carrier Diodes in Guide

guide as well as from one another. Insulation from the guide is achieved by means of 1.0-mil Mylar tape which also serves as the dielectric for the capacitance introduced between each output terminal and the guide. This capacitance, which amounts to about 100 pF in each leg, serves as an output filter for securing low ripple.

Beyond the diode array in the guide is an adjustable tuning short which allows an additional degree of freedom in securing a match.

An 8-GHz version of essentially the same design is shown in the photograph in Figure 50. This rectifier is fabricated from RG-52/U waveguide.

Typical results of efficiency measurements at 4 GHz are shown in Figures 53 through 56. Figures 53 and 54 show the effect of different load resistance plotted as a function of input power for bridges having diodes of two different areas.

Despite the fact that these area ratios are 2:1, very little difference between the two sets of data is seen. The load resistance has a pronounced effect on the shape of the efficiency versus input power curves but does not have much effect on the maximum efficiency achievable.

The shape of the curves shown in Figures 53 and 54 can be qualitatively understood in terms of the competition between the power loss due to the forward drop of the diode and that due to reverse breakdown. The higher the load resistance, the larger is the output voltage required to achieve a given output power. Since the reverse voltage seen by each diode is nearly equal to the output voltage, the devices can be expected to break down at lower input power for higher load resistances.

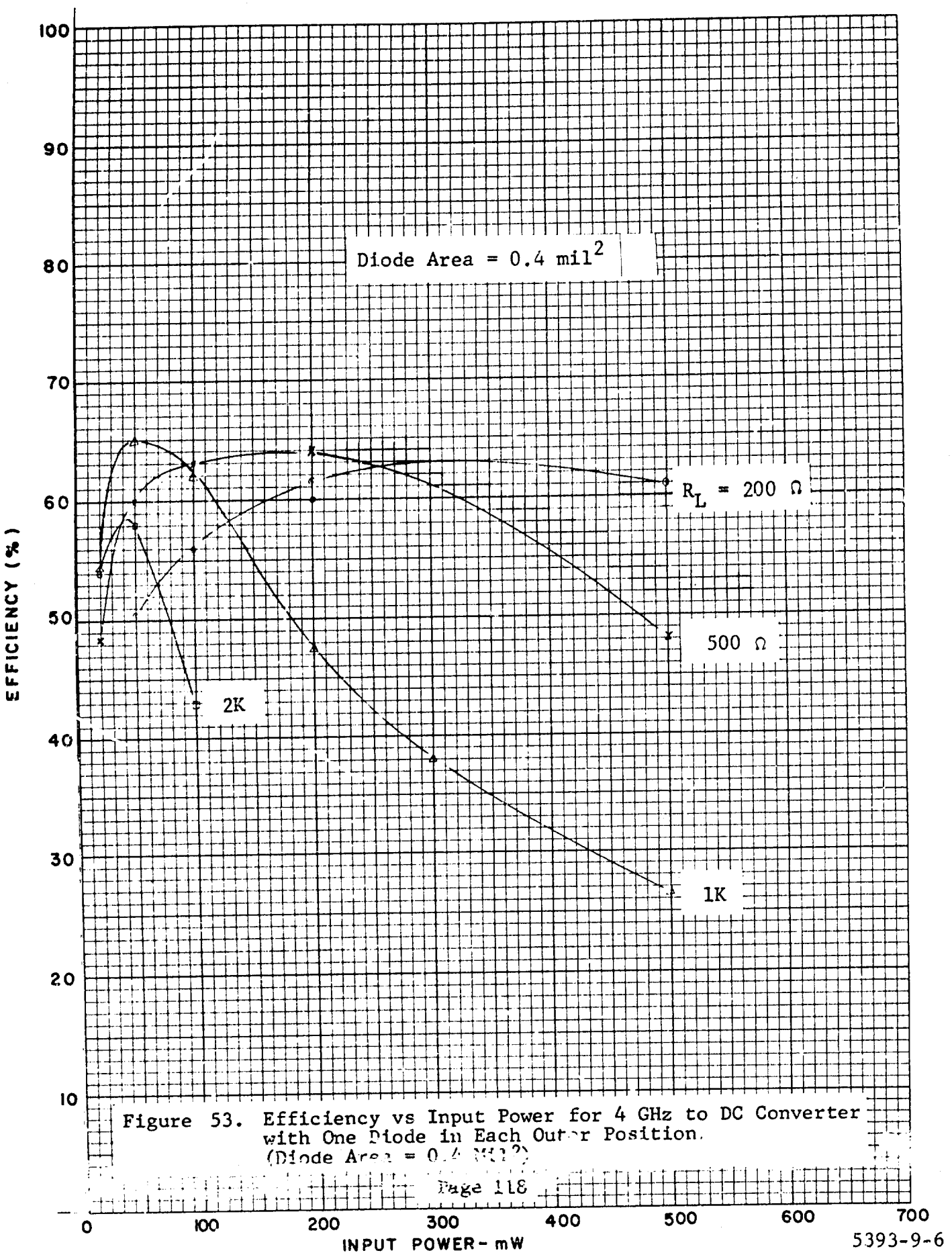


Figure 53. Efficiency vs Input Power for 4 GHz to DC Converter with One Diode in Each Outer Position. (Diode Area = 0.4 mil^2)

5393-9-6

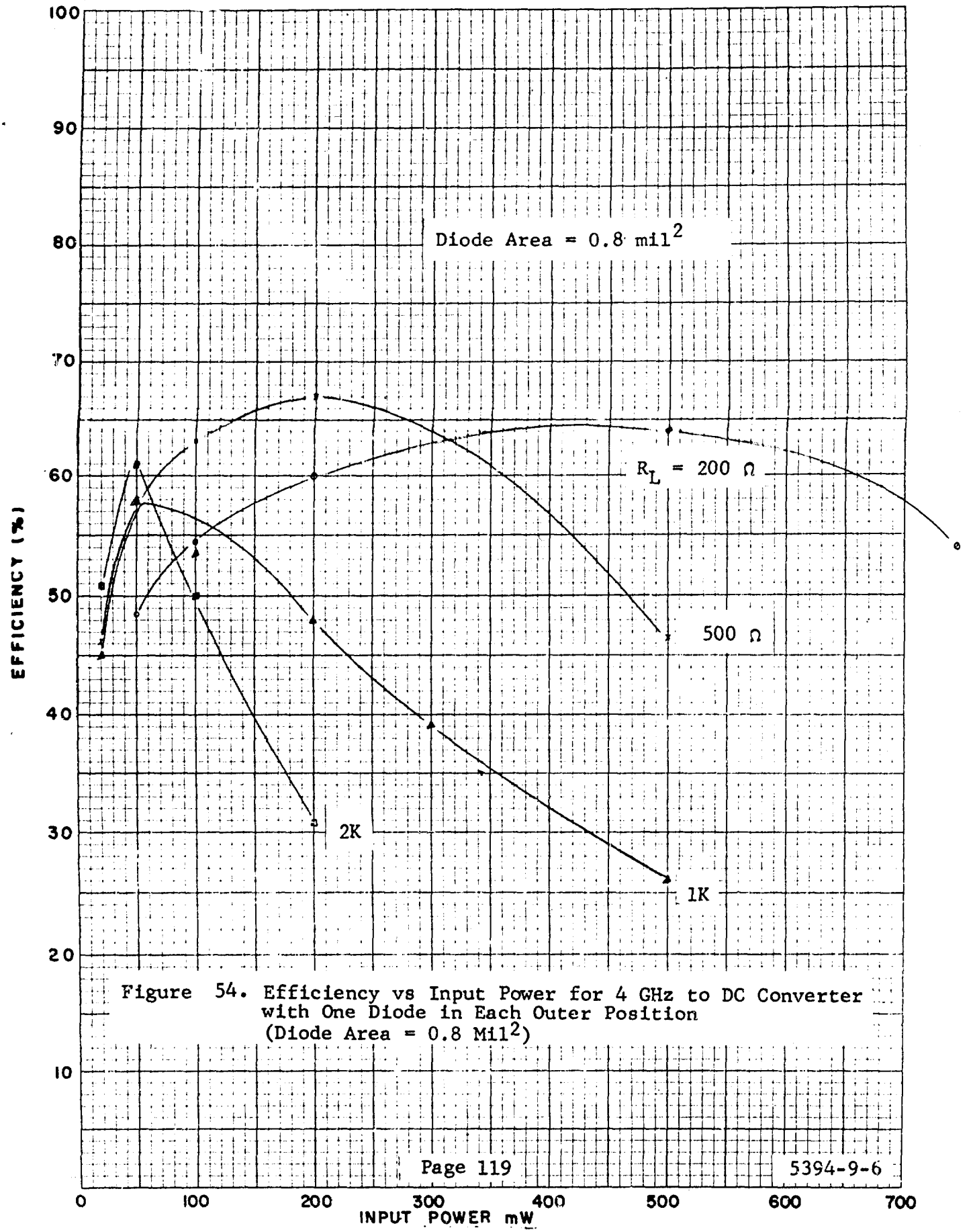


Figure 54. Efficiency vs Input Power for 4 GHz to DC Converter with One Diode in Each Outer Position (Diode Area = 0.8 Mil^2)

5394-9-6

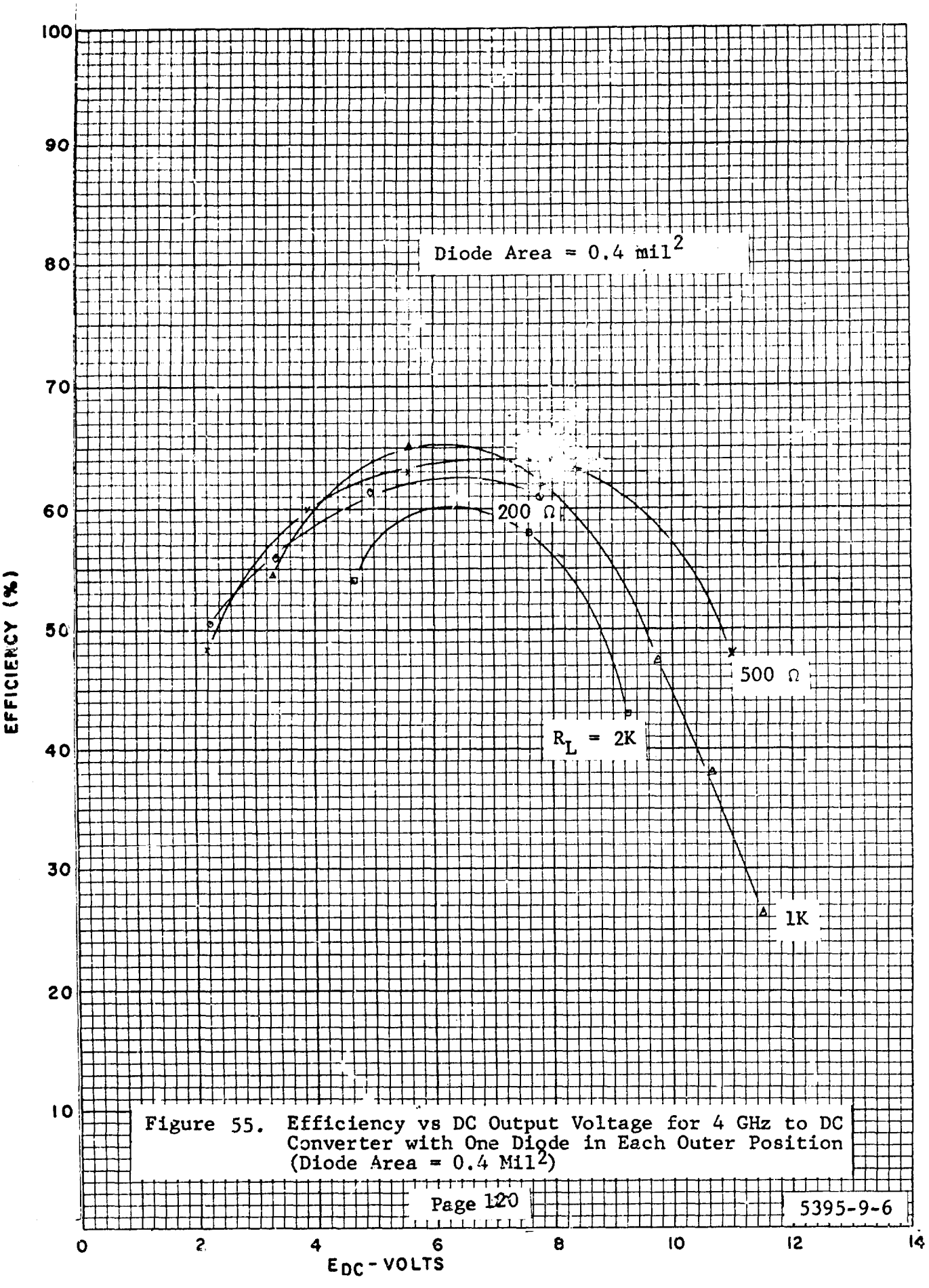


Figure 55. Efficiency vs DC Output Voltage for 4 GHz to DC Converter with One Diode in Each Outer Position (Diode Area = 0.4 Mil^2)

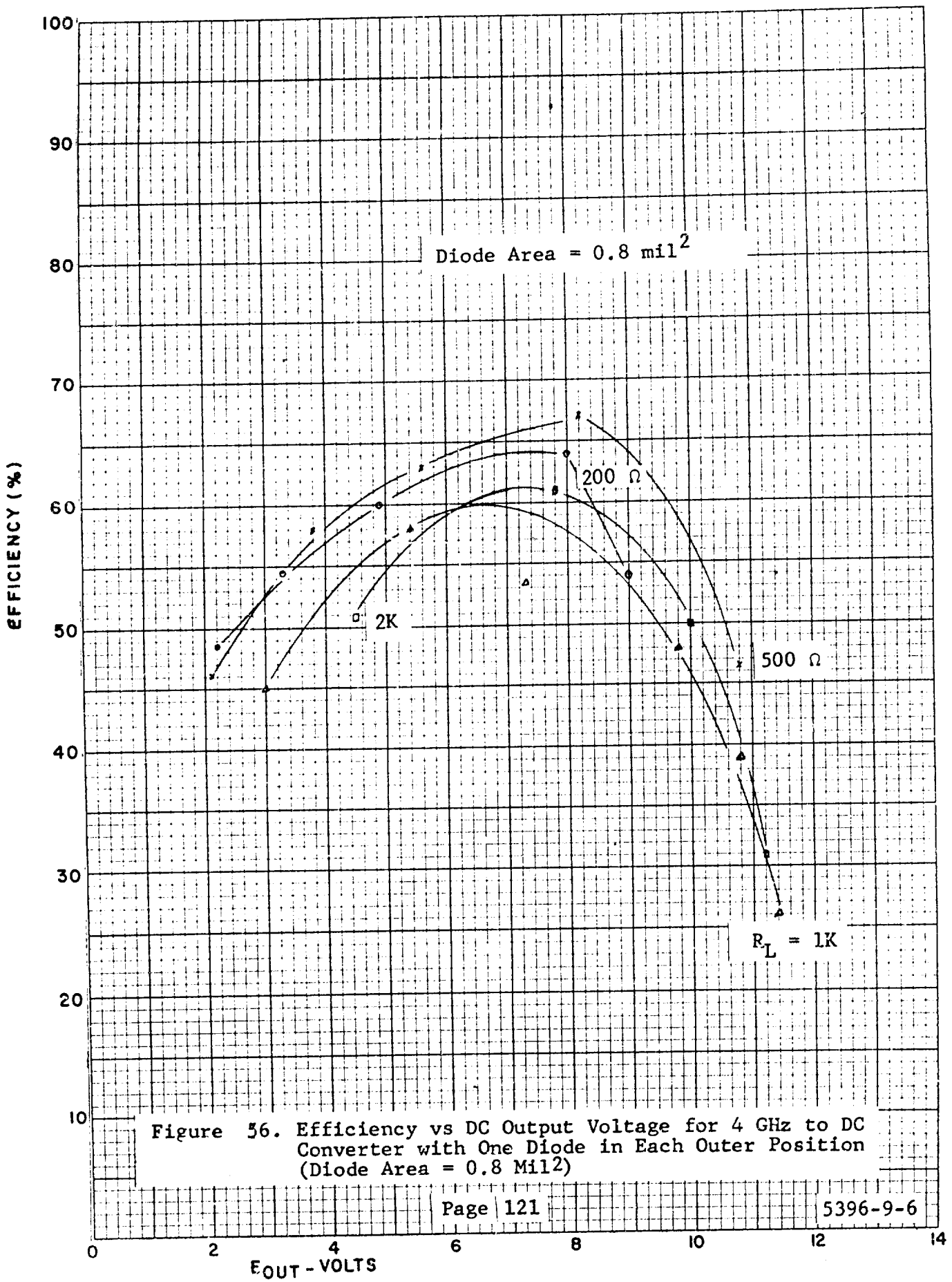


Figure 56. Efficiency vs DC Output Voltage for 4 GHz to DC Converter with One Diode in Each Outer Position (Diode Area = 0.8 Mil2)

Further evidence for this interpretation is seen in Figures 55 and 56 where efficiency is plotted as a function of output voltage. The curves for different load resistance all have similar shape and tend to nest rather close to one another, the efficiency falling rather rapidly for output voltages of 9 to 11 volts, which is the approximate range of breakdown voltages for the diodes used in the test.

Measurements made on the 8-GHz bridge gave similar results to the 8-GHz measurements made with the half-wave coaxial circuit described in the next subsection.

7.4 HALF-WAVE RECTIFIER

Figure 57 shows a cross section of the half-wave fixture. It consists of a type N coupling which has been modified to allow the mounting of a single diode in a pill package, in series with the center conductor. The mating part carries a large diameter solid brass inner conductor, insulated from the outer conductor by 1.0-mil Mylar, which contacts the other end of the diode package, thus providing an effective shunt capacitance output filter.

Figures 58 through 61 show efficiency data at different frequencies for one of the best diodes which we have produced. It can be seen that at the lower frequencies the behavior is quite similar to that obtained with the 4-GHz full-wave bridge circuit, while at the higher frequencies there does not appear to be as much falloff in efficiency with input power, at least out to 400 mW.

In Figure 62, we have plotted the efficiency as a function of frequency for given input power and load resistance and it is seen that a dip exists at about 6 GHz. This is not a

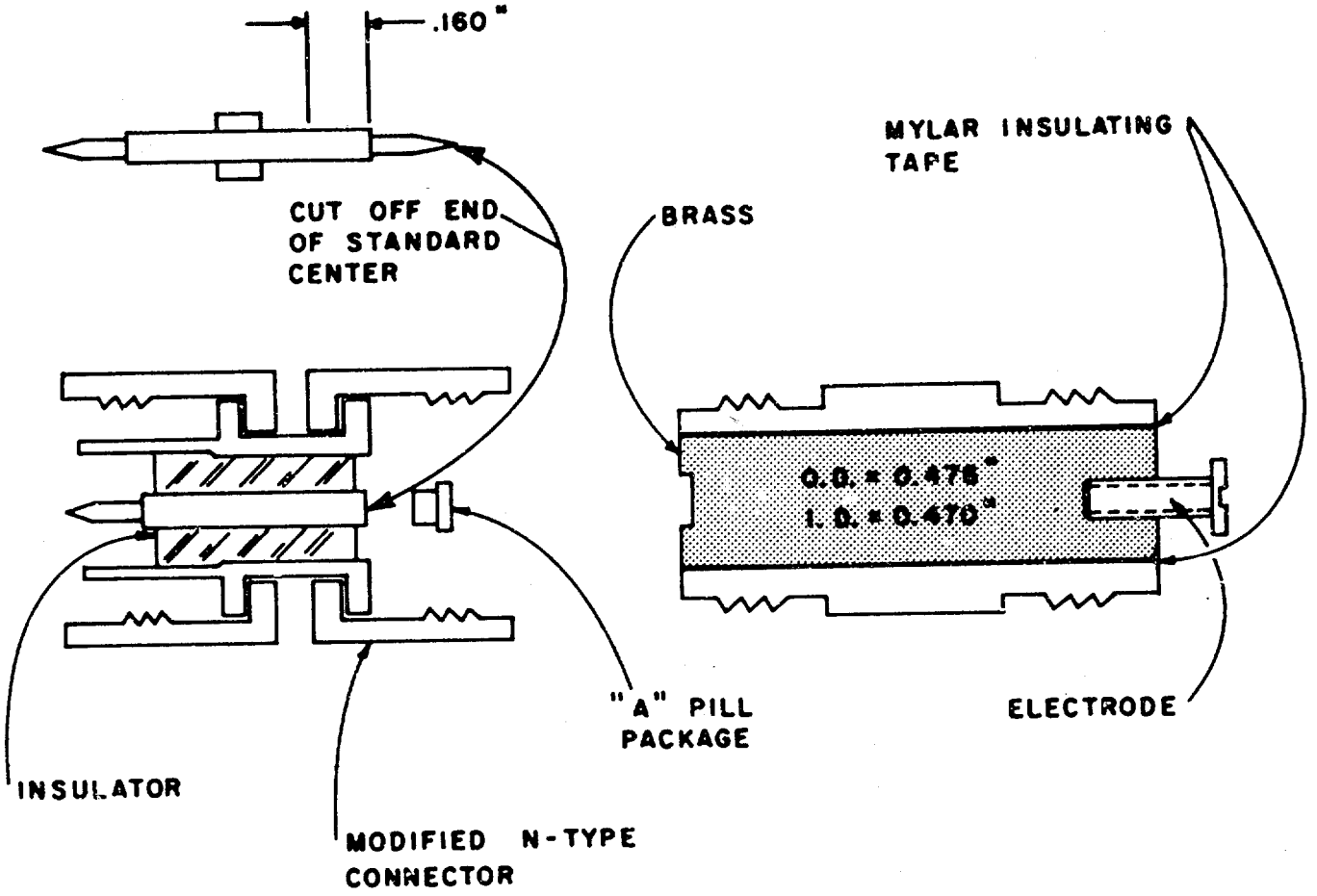


Figure 57. Half-Wave Rectifier Test Fixture

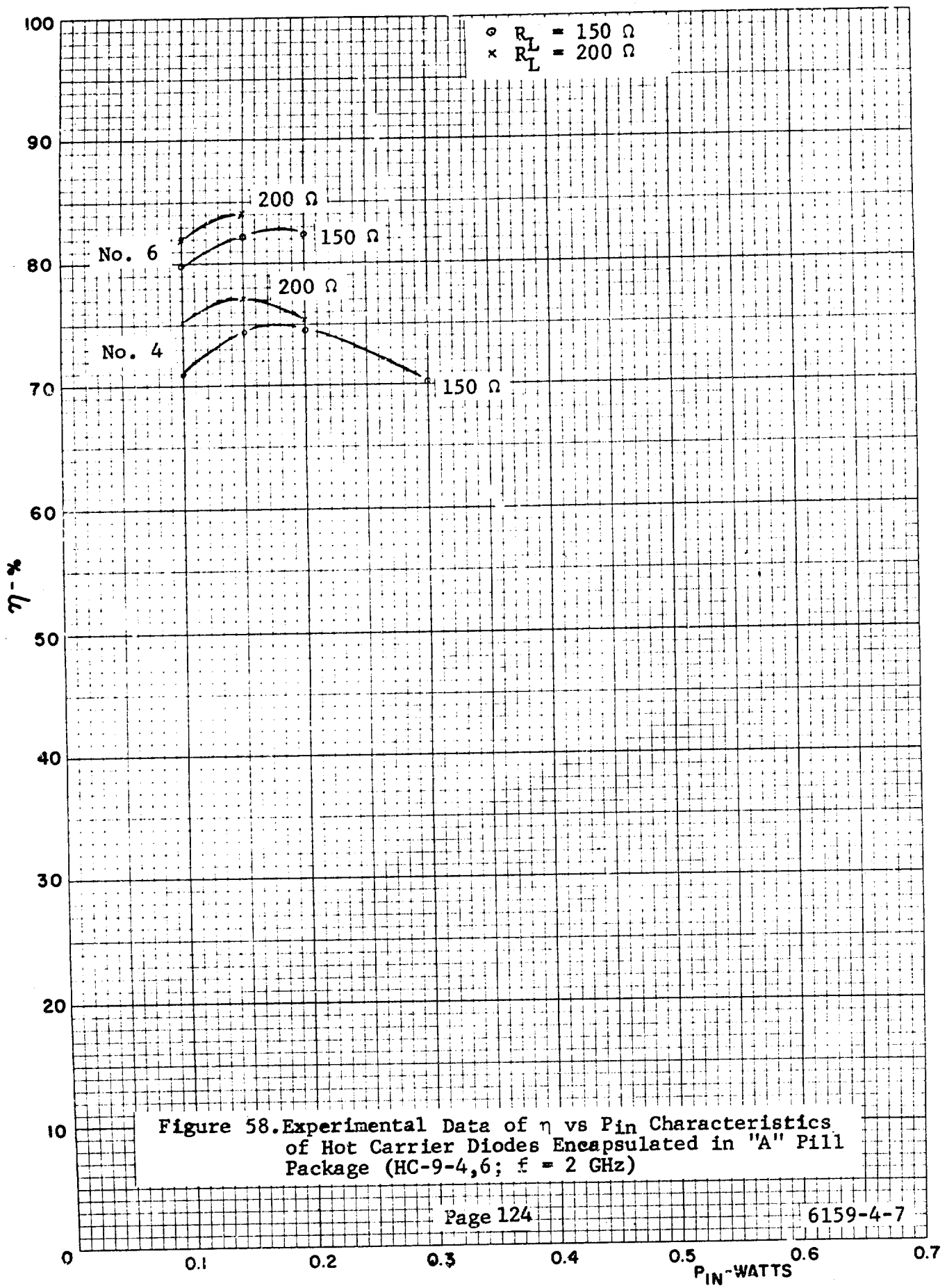


Figure 58. Experimental Data of η vs P_{in} Characteristics of Hot Carrier Diodes Encapsulated in "A" Pill Package (HC-9-4,6; f = 2 GHz)

6159-4-7

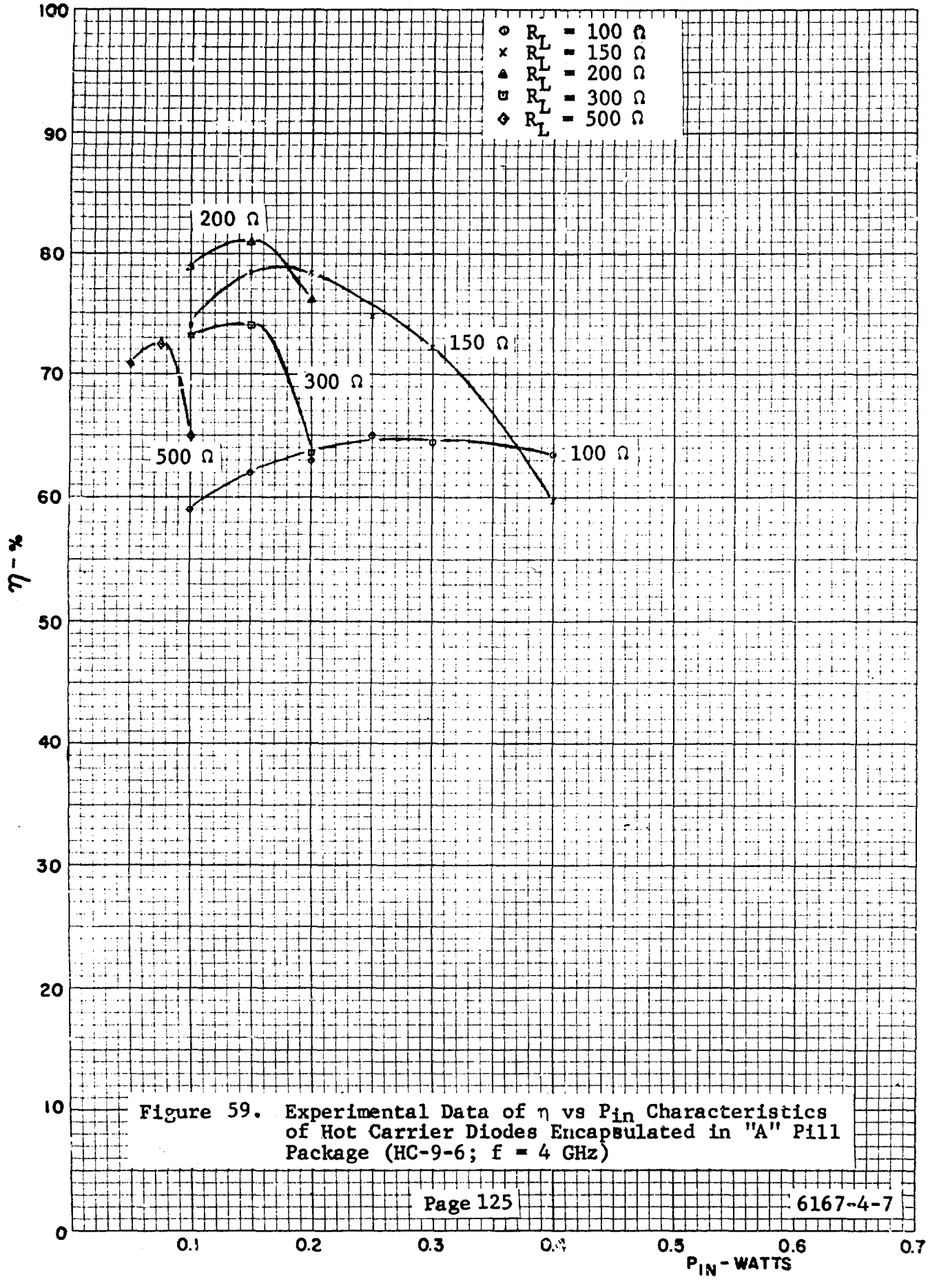


Figure 59. Experimental Data of η vs P_{in} Characteristics of Hot Carrier Diodes Encapsulated in "A" Pill Package (HC-9-6; f = 4 GHz)

6167-4-7

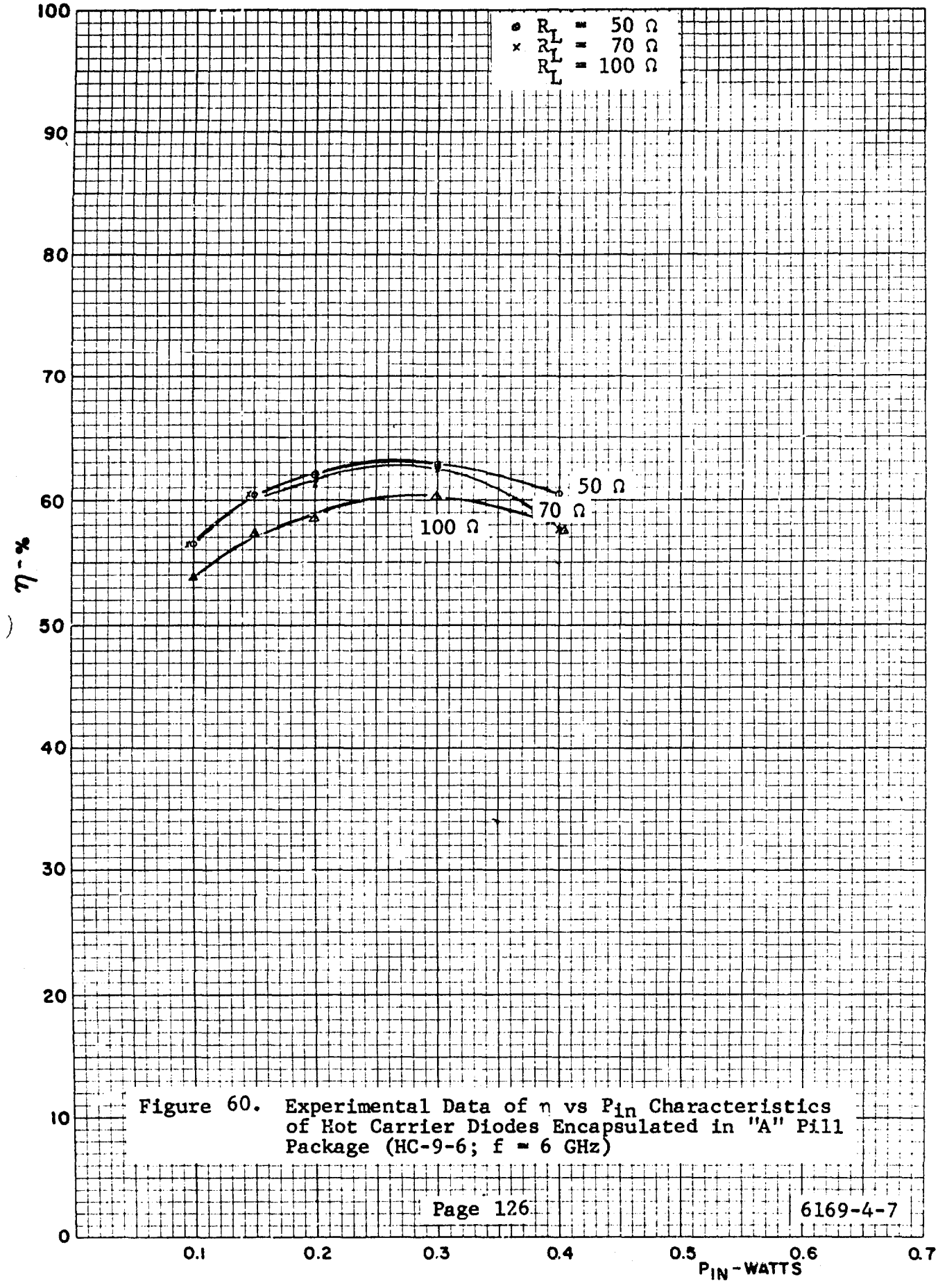


Figure 60. Experimental Data of η vs P_{in} Characteristics of Hot Carrier Diodes Encapsulated in "A" Pill Package (HC-9-6; f = 6 GHz)

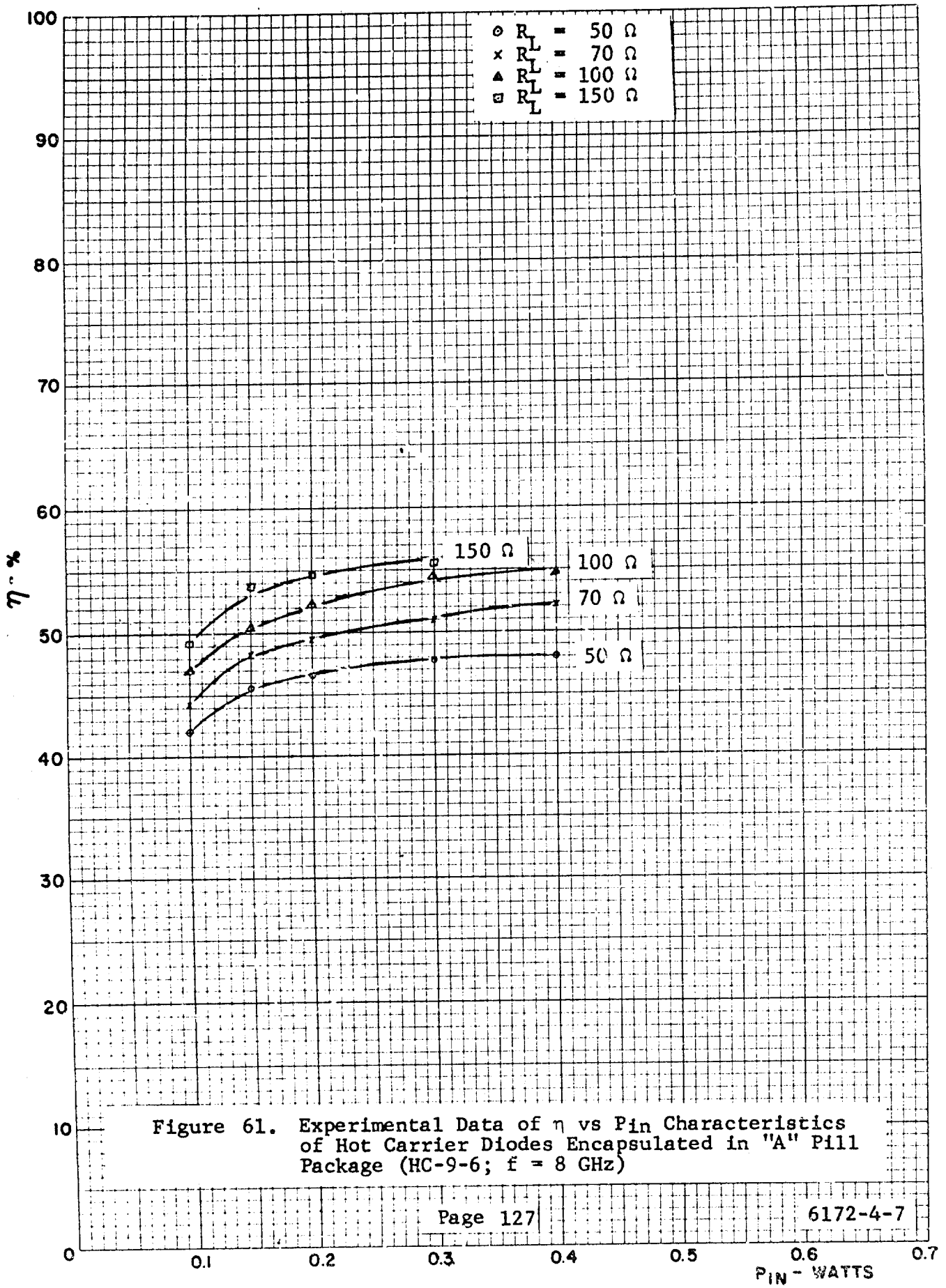


Figure 61. Experimental Data of η vs Pin Characteristics of Hot Carrier Diodes Encapsulated in "A" Pill Package (HC-9-6; f = 8 GHz)

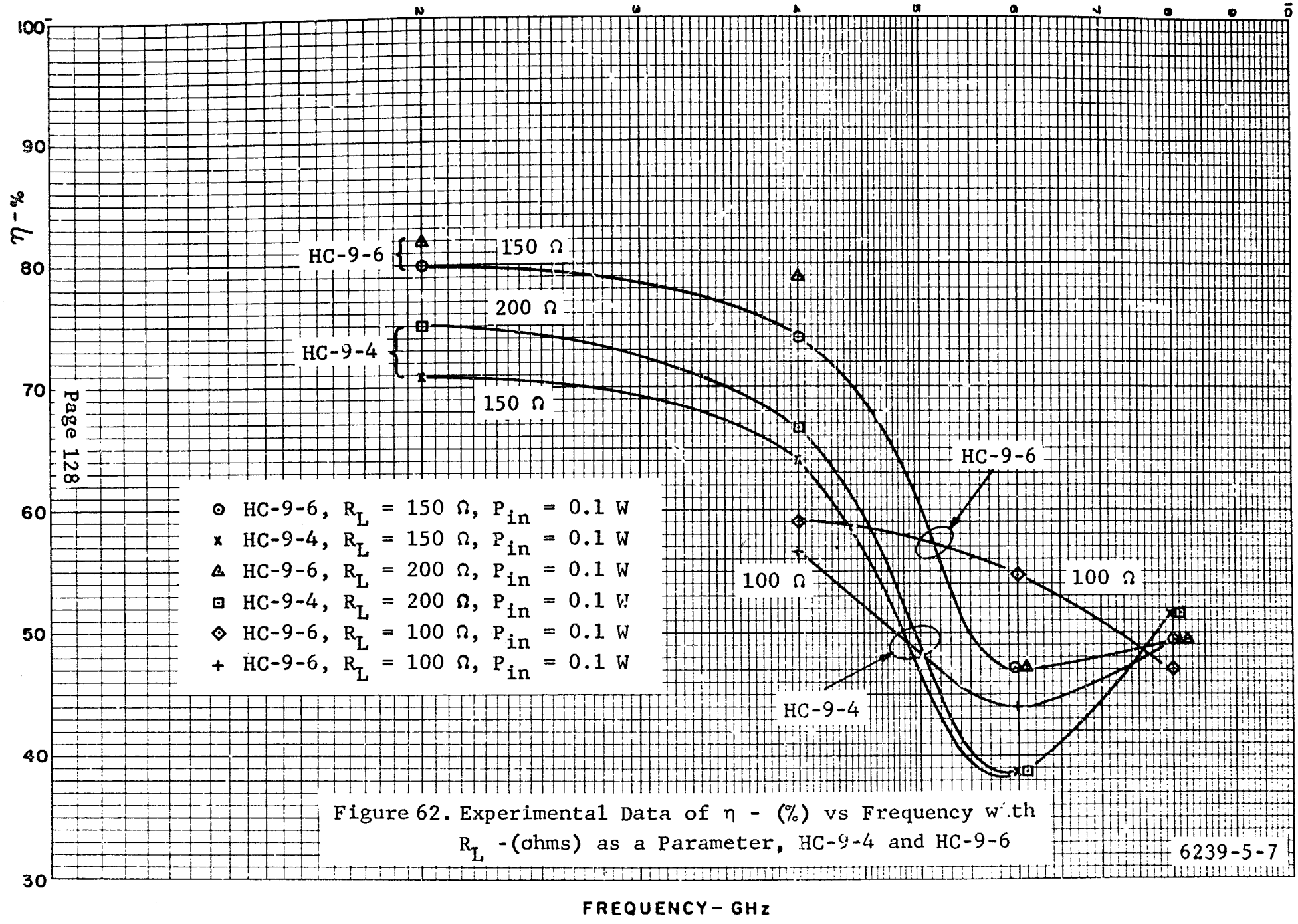


Figure 62. Experimental Data of η - (%) vs Frequency with R_L -(ohms) as a Parameter, HC-9-4 and HC-9-6

fundamental diode characteristic but is due rather to the fact that we were unable to secure an adequate match at this frequency because of the limitation of the double stub tuner used. Thus, a significant reflected power was indicated at 6 GHz and this measurement is somewhat in error. This problem was overcome by using an E-H plane tuner in place of the double stub at the higher frequencies and a substantial increase in efficiency was noted. This data is presented in a following subsection.

In Figure 63 we have an example of the qualitative change in the shape of the efficiency vs input power curves as a result of using a diode having a higher breakdown voltage, in this case 20 volts. Instead of the rapid falloff in efficiency previously noted at 4 GHz we find a shallow maximum followed by a relatively flat curve, thus showing that the falloff is definitely associated with diode breakdown.

The somewhat lower efficiency observed in Figure 63 is a result of a higher forward drop, V_F, for the higher breakdown diode in comparison with the 10-volt diodes. This points up one of the difficulties we have encountered in attempting to improve the efficiency of our diodes, in that very little improvement seems possible in the ratio of breakdown voltage to forward drop.

7.5 FULL-WAVE BALANCED STRIPLINE CIRCUITS

A total of four stripline circuits were fabricated for operation at frequencies between 1 and 8 GHz. Three of these were included on the same substrate board to simplify the overall fabrication procedures.

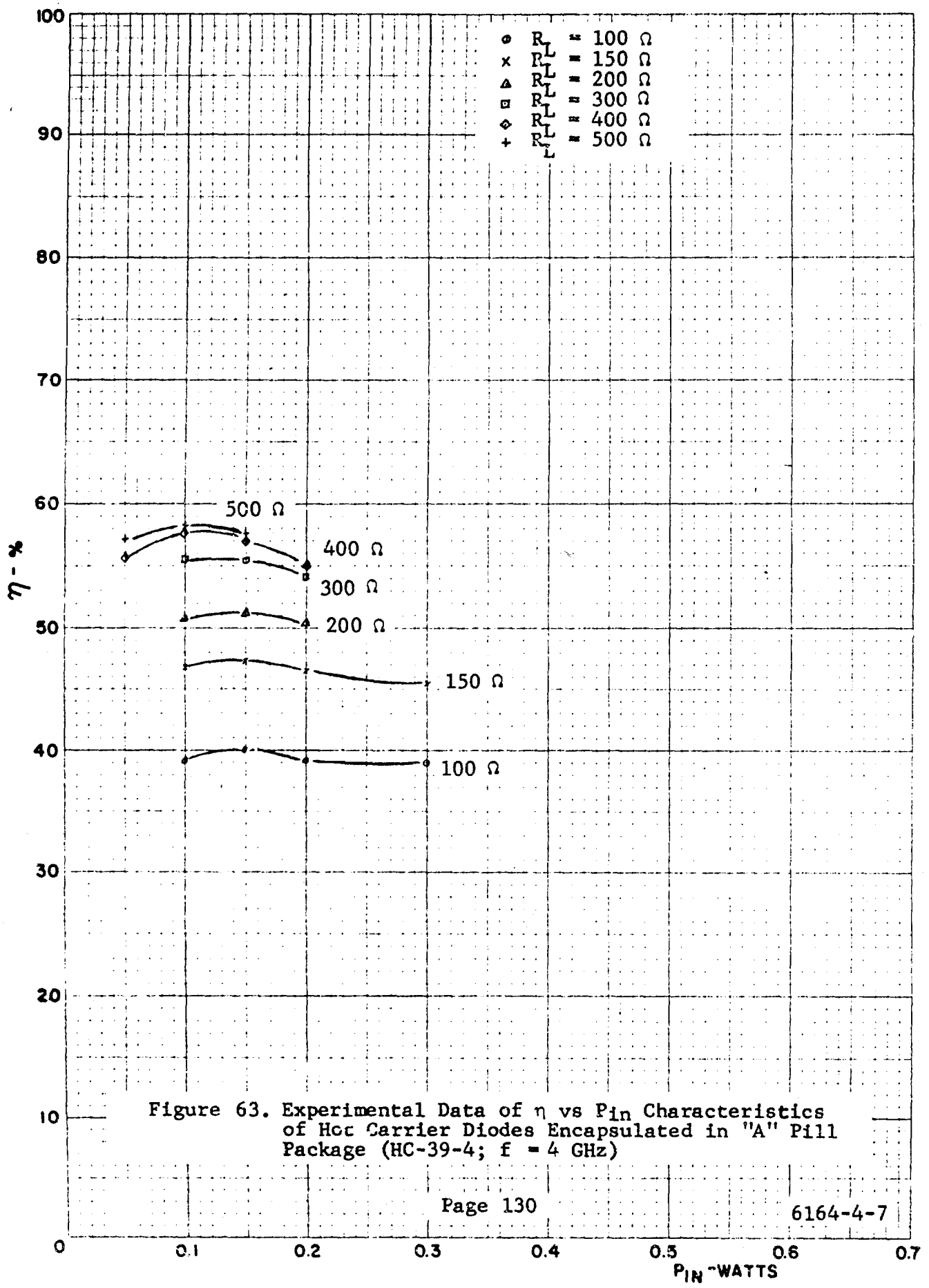


Figure 63. Experimental Data of η vs P_{in} Characteristics of Hot Carrier Diodes Encapsulated in "A" Pill Package (HC-39-4; f = 4 GHz)

A schematic diagram for the 1-GHz circuit is shown in Figure 64 and the actual converter is shown in the photographs of Figure 65. The balanced arrangement consists of two 100-ohm transmission lines emanating from a 50-ohm input line in a power divider arrangement, with the diodes mounted at the ends of the 100-ohm lines so that they are one-half wavelength apart at the fundamental frequency.

A harmonic "T" filter section is provided at the input to prevent the absorbtion of harmonics by the source, and an RF choke is provided to supply a dc return for the diodes.

Efficiency measurements made at 1 GHz, the frequency at which the diodes are one-half wavelength apart, yielded results a few percent lower than those obtained with the half-wave coaxial circuit. The reason for the slightly lower figure is not known. It was originally felt that this circuit should be somewhat better than either the half-wave or full-wave bridge since in operation it is similar to the latter but involves conduction through only a single diode at a time, thus reducing the effect of the forward losses in the diodes. In practice however, this does not seem to be the case.

Photographs in Figures 66 and 67 show the combined 4, 6, and 8 GHz balanced stripline circuits. Each section of the converter is essentially the same as the 1-GHz model except that no input filtering is included. Thus, the harmonic rejection depends upon the matching tuner used on the input during measurements, just as in the case of the full-wave bridge and half-wave circuits.

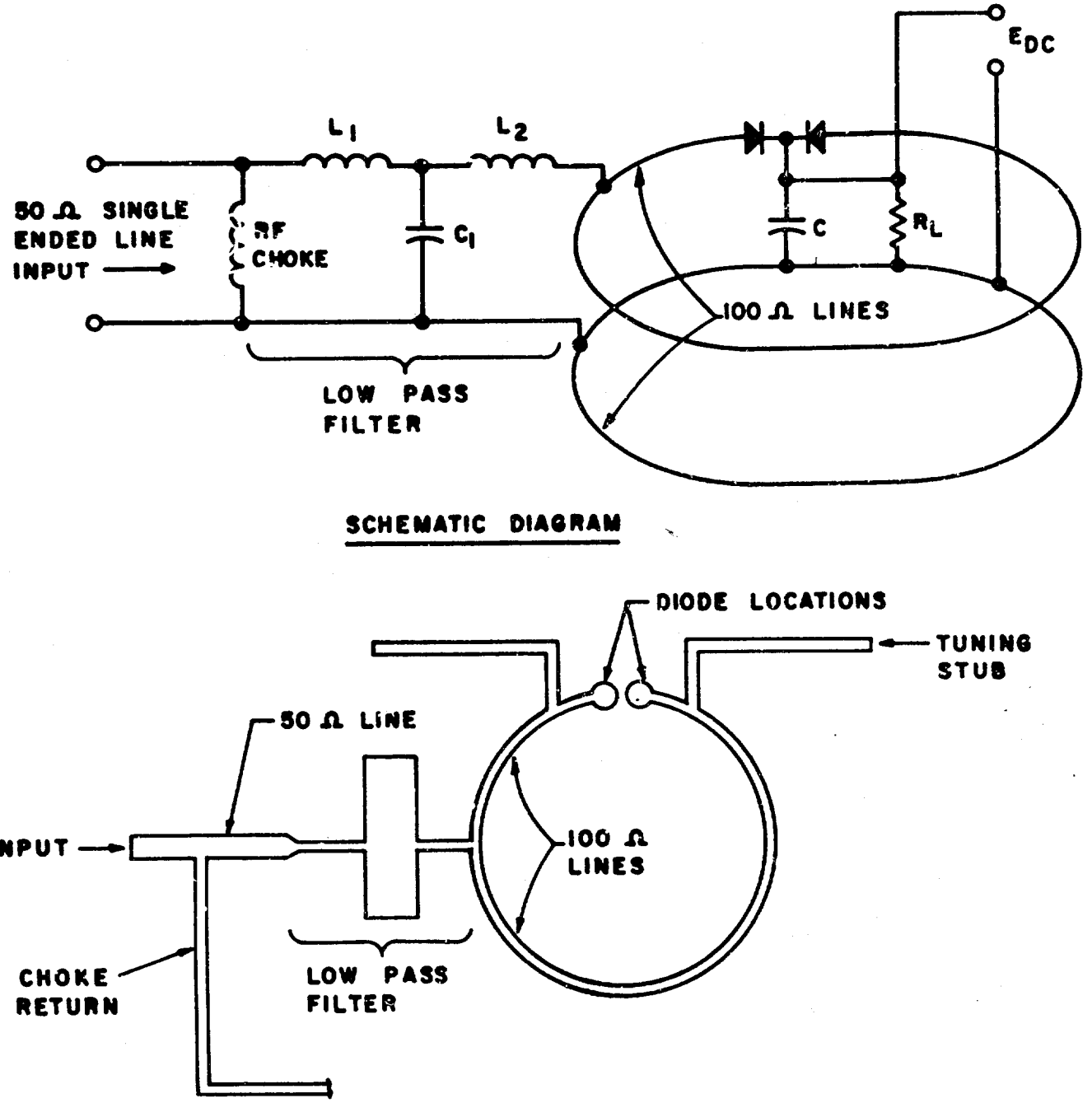


Figure 64. 1-GHz Balanced Stripline RF to DC Converter

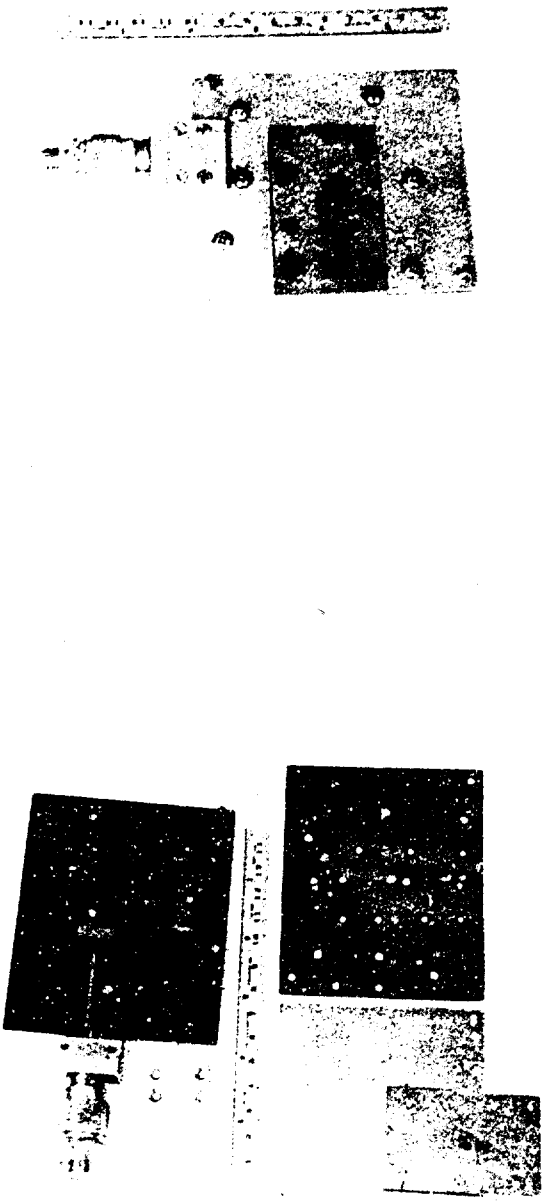


Figure 65. 1-GHz Balanced Stripline RF to DC Converter Assembled and Disassembled

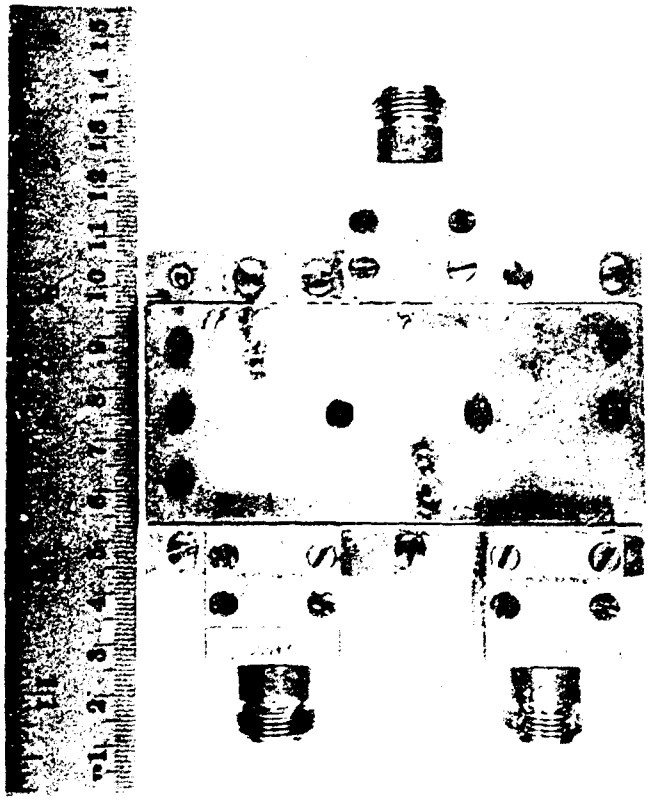
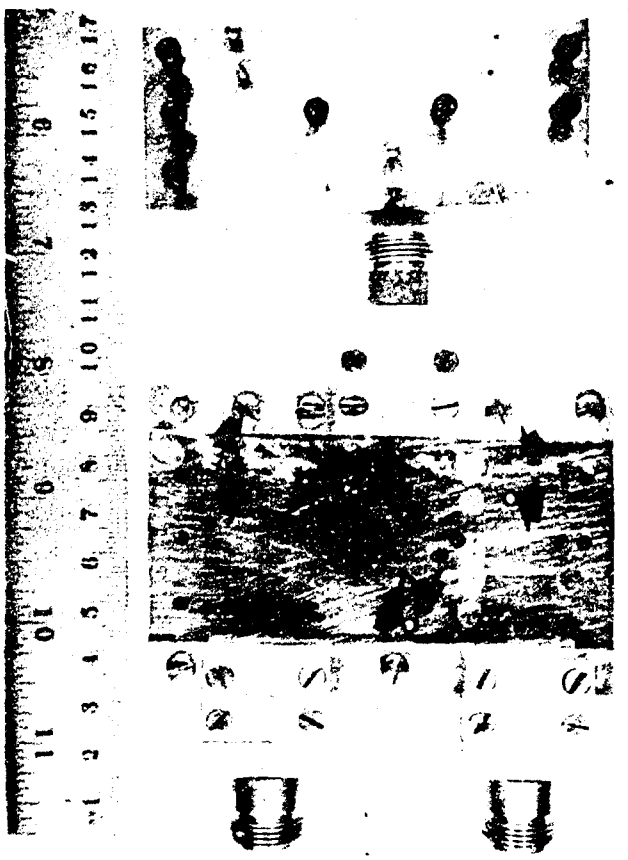


Figure 66. Stripline Circuit Fully Assembled



NOTE: Diodes are indicated by black arrows on photo

Figure 67. Stripline Circuit Partially Dismantled Showing Diodes

This converter was not completed until the very end of the contract so that only a few tests were made with it. The results of these showed that the 4-GHz section works well at that frequency, giving about the same efficiency as the half-wave circuit, while the 6-GHz section appears to produce maximum efficiency closer to 5 GHz, this efficiency being a bit lower than that obtained with the half-wave circuit. Equipment difficulties at the end of the contract period prevented us from making tests at 8 GHz.

7.6 SUMMARY OF RESULTS OBTAINED ON 100 HOT CARRIER DIODES

In this subsection a summary of the final test results obtained on the 100 hot carrier diodes fabricated as a partial requirement for this contract is presented. The efficiency measurements were made with the circuit of Figure 49 described at the beginning of this section, using the half-wave test fixture. At 4 GHz the double-stub tuner was used to obtain a match while at 8 GHz this was replaced by an E-H plane tuner.

Figure 68 shows some typical results at these two frequencies. Here we see that at low powers the efficiency is greater at 8 GHz than at 4 GHz. This unusual result is probably due to the difference in insertion loss between the two tuners used. As mentioned earlier, this loss has been observed to vary considerably with VSWR.

A probability plot of the data for the 100 diodes is given in Figure 69 where the percentage of diodes having efficiency greater than a given value is plotted against the efficiency. Thus, all diodes have an efficiency greater than 50 percent at both 4 and 8 GHz, while 27 percent have an efficiency greater than 70 percent at 4 GHz and only about 2½ percent have an efficiency greater than 70 percent at 8 GHz.

Surprisingly, the falloff in efficiency with frequency is rather small so that more than half of the diodes have an efficiency greater than 60 percent at 8 GHz.

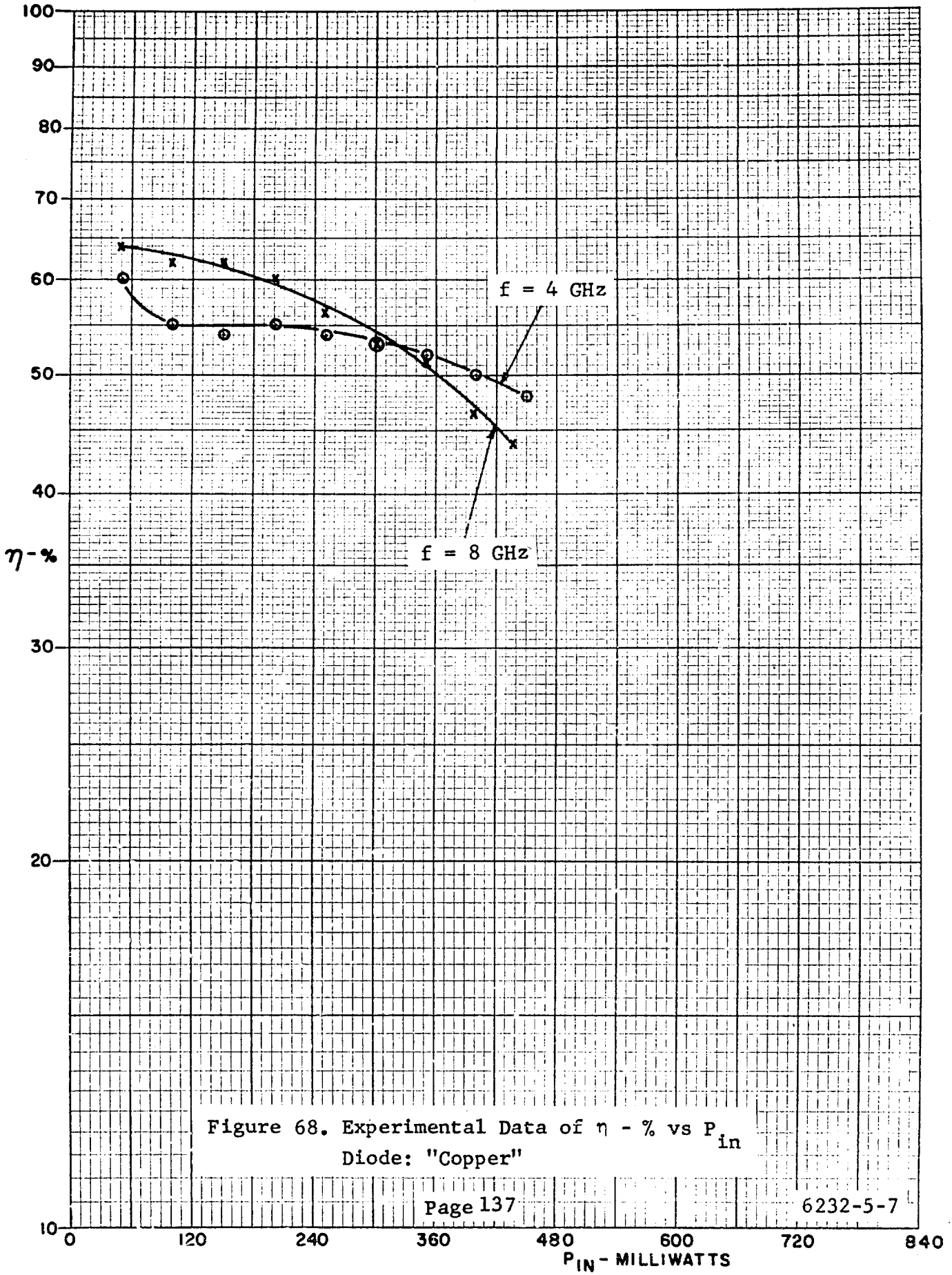


Figure 68. Experimental Data of η - % vs P_{in}
Diode: "Copper"

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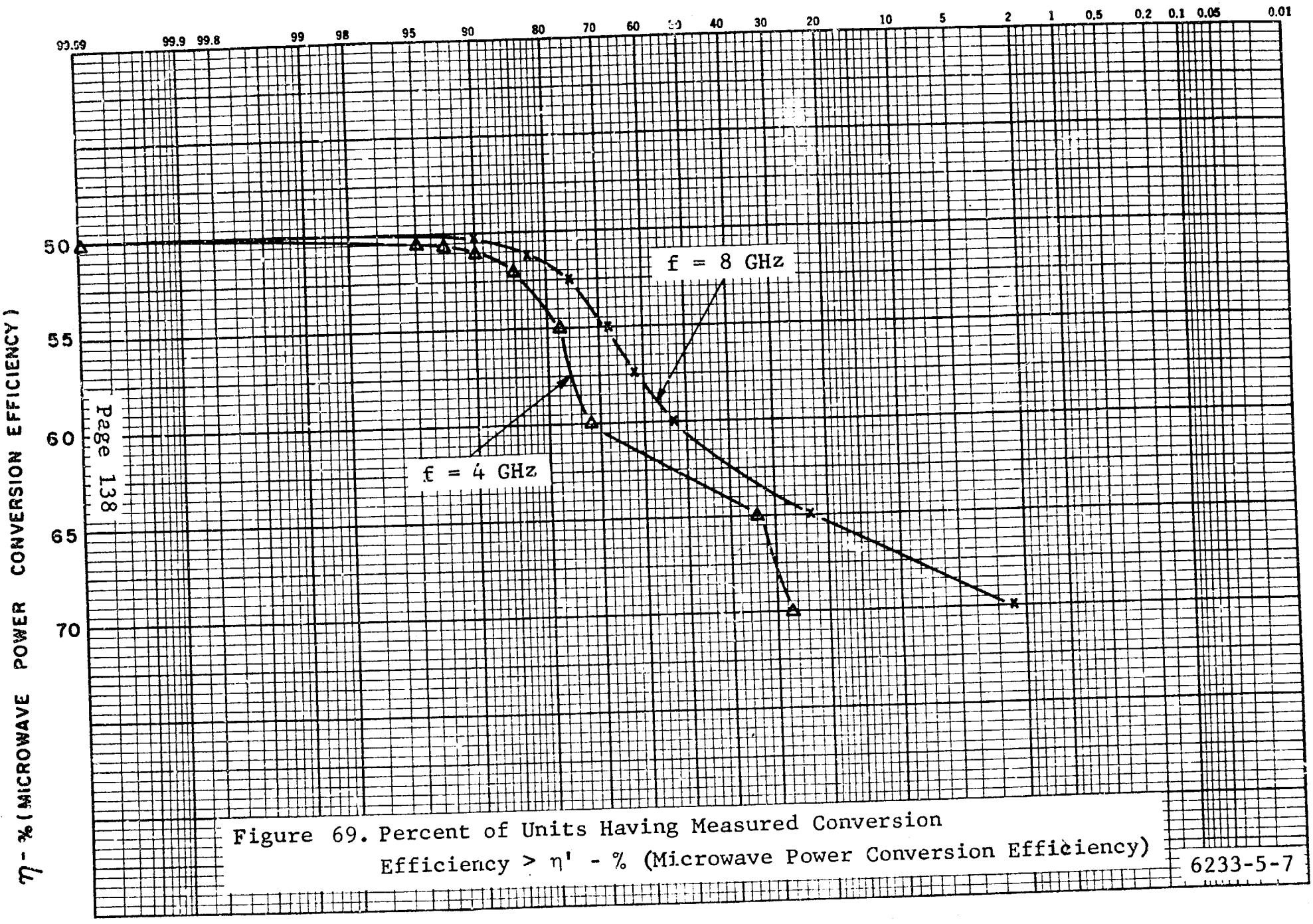

Figure 69. Percent of Units Having Measured Conversion Efficiency > η' - % (Microwave Power Conversion Efficiency)

6233-5-7

SECTION VIII

8.0 SUMMARY AND CONCLUSIONS

A theoretical analysis of the fundamental aspects of the rectification process has shown that high efficiency operation can only be achieved by using suitable filtering between the source and rectifier to prevent losses due to harmonic absorption at the source.

In practice, at microwave frequencies it is difficult to provide special lossless filtering and we have, in general, depended upon the tuner, which is required at the input to provide a correct match, to act as a filter also. Thus, one does not have independent control over the harmonics, except in that the tuning procedure minimizes the total reflected power, including harmonics, and this is usually observed to be less than 1 percent.

The current and voltage waveforms for the rectifier are completely unknown at these frequencies so that actual loss calculations are impossible. One exception to this is the loss due to V_F, discussed in Section 2, which was shown to be independent of the waveform and dependent only upon the dc output voltage, E_{DC}. Typically, this amounts to a loss of from 10 to 20 percent, depending upon which circuit is used (full-wave bridge or half-wave).

It is felt that any future effort to improve the rectification efficiency should involve further attempts at lowering the forward voltage drop at high currents and a program aimed at a more complete understanding of the high frequency equivalent circuit for the hot carrier diode.

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13. ABSTRACT

The purpose of this contract was to investigate the problem of high efficiency microwave rectification with hot carrier diodes and to provide diodes having the highest efficiency possible in the frequency range of 3 to 8 GHz. A theoretical analysis is first made of the problem from the circuit viewpoint in an effort to determine which rectifier configurations should produce optimum efficiency, assuming perfect diodes. This is followed by an analysis of the losses to be expected for various circuits on the basis of a given diode equivalent circuit. Details of diode design, fabrication and characterization are followed by low and intermediate frequency efficiency measurements, where an attempt to correlate results obtained with the theory is made. Finally, efficiency measurements at microwave frequencies are described, including those made on 100 diodes fabricated for delivery at the conclusion of the contract.

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14 KEY WORDS	LINK A		LINK B		LINK C	
	ROLE	WT	ROLE	WT	ROLE	WT
Rectification efficiency						
Electron beam evaporation						
Sputtering						
Microwave						
Lifetime						
Full-wave rectifier circuit						